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vSuperb_-1

Schematics Document

Haswell LGA1150

Intel Lynx Point

BOM Configuration

| | H81 | Q87 |
|------------------------------|------------|------------|
| A: AMP | X | X |
| N: No AMP | V | V |
| G: G-sensor | V | V |
| U: UMA - Non Scalar | V | X |
| S: Scalar | X | V |
| L: Internal DP for 1L | X | X |
| R: Unmount | | |

PCB BOARD SIZE
8 Layers
170mm X 170mm

Schematics change

SA —
SB —
IA —
-1 —

| | | | |
|---------------|---------------------------|--|---------|
| <Core Design> | | | |
| 緯創資通 | | Wistron Corporation | |
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| Cover Page | | | |
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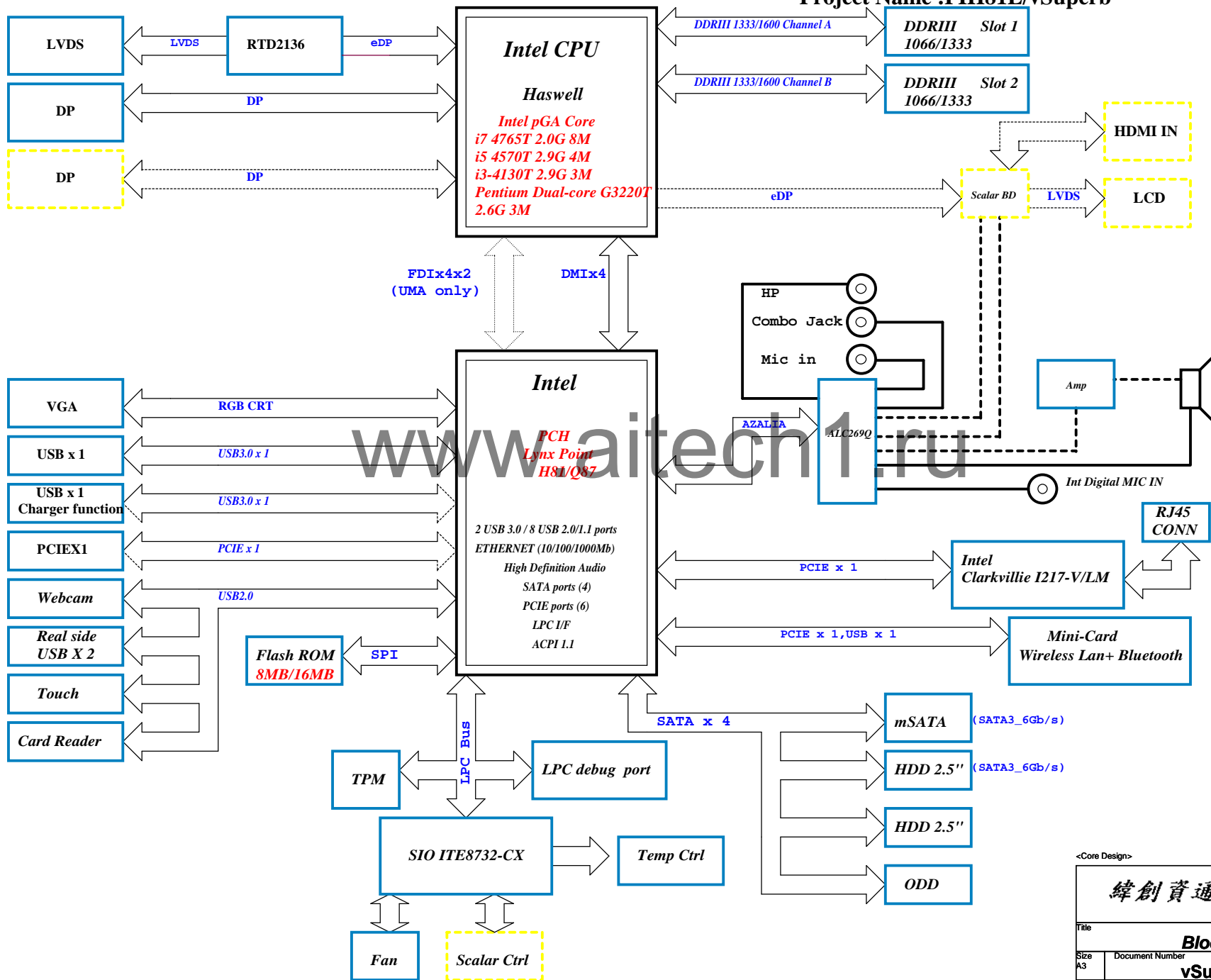
Swift Block Diagram

Project code :91.3KB01.001

PCB No :13045

Revision :-1

Project Name :PIH81L/vSuperb



| BATTERY CHARGER | |
|-----------------|----------|
| BQ24727RGRR 49 | |
| INPUTS | OUTPUTS |
| ADP+ | DCBATOUT |

| SYSTEM DC/DC | |
|--------------|--|
| TPS51225 50 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_AUX_S5 3D3V_AUX_S5 5V_A 3D3V_A |

| CPU DC/DC | |
|-------------------|----------|
| ISL95812HRZ 51-52 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE |

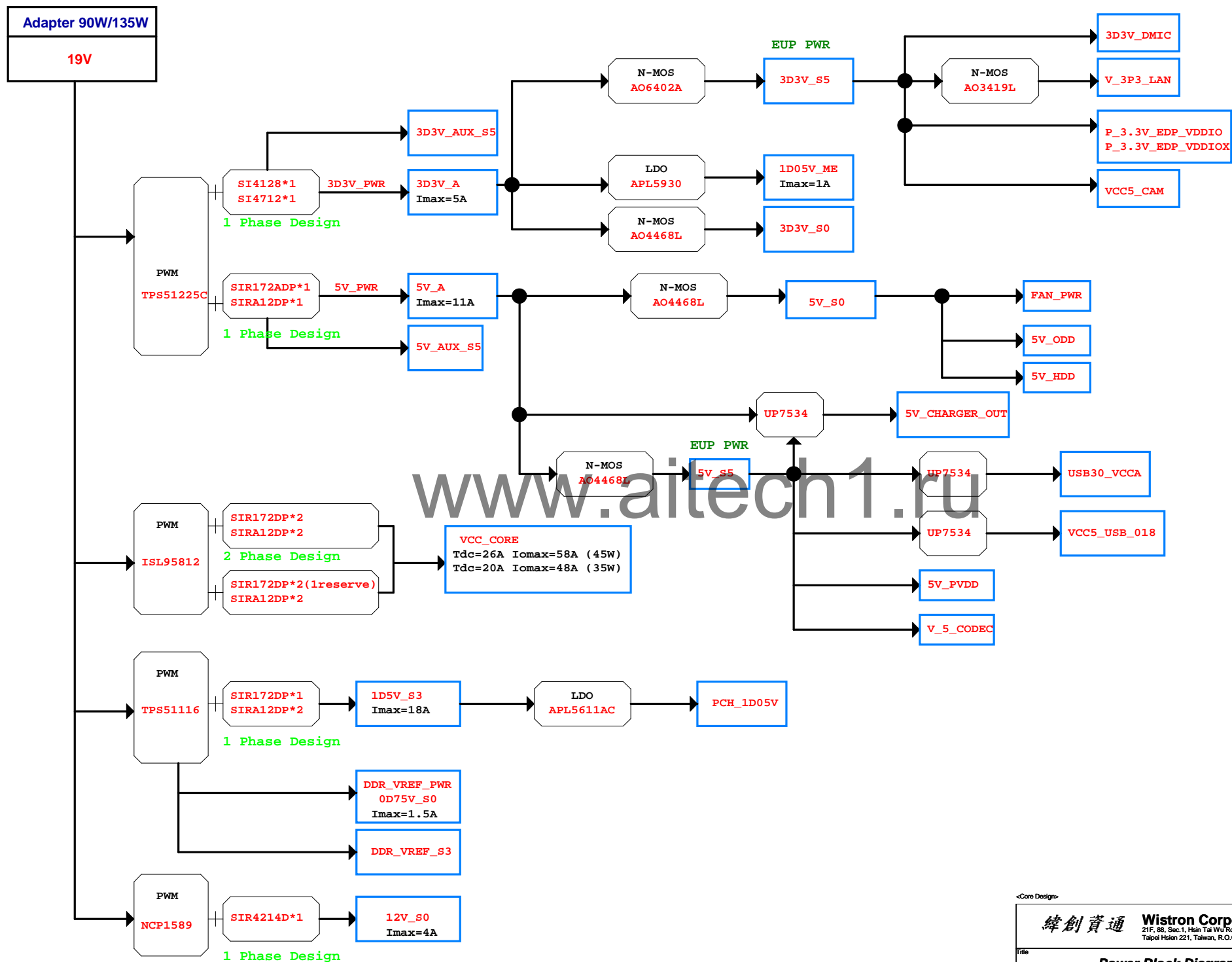
| SYSTEM DC/DC | |
|--------------|------------------------------------|
| TPS51116 53 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D5V_S3 0D75V_S0 DDR_VREF_S3 |

| LDO | |
|---------------|-----------|
| APL5611ACI 54 | |
| INPUTS | OUTPUTS |
| 12V_S0 | PCH_1D05V |

| LDO | |
|---------------|----------|
| APL5930KAI 54 | |
| INPUTS | OUTPUTS |
| 3D3V_A | 1D05V_ME |

| SYSTEM DC/DC | |
|------------------|---------|
| NCP1589AMNTWG 55 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 12V_S0 |

| PCB LAYER | |
|-----------|-----------|
| L1:Top | L5:VCC |
| L2:GND | L6:Signal |
| L3:Signal | L7:GND |
| L4:Signal | L8:Bottom |



<Core Design>

緯創資通

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Title

Power Block Diagram

Size

Document Number

vSuperb

Rev

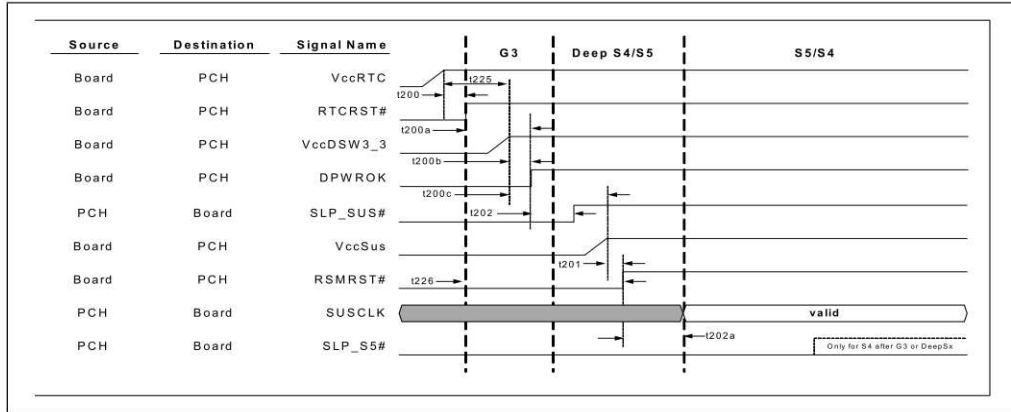
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Date: Tuesday, October 08, 2013

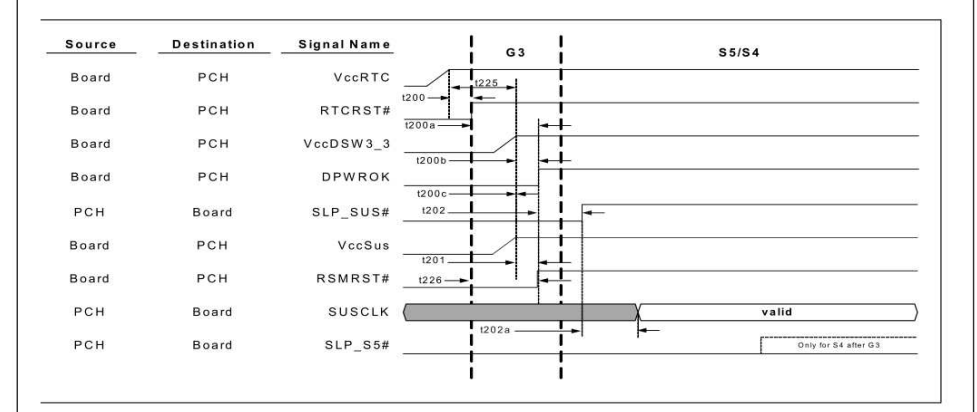
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Power Sequence

G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram

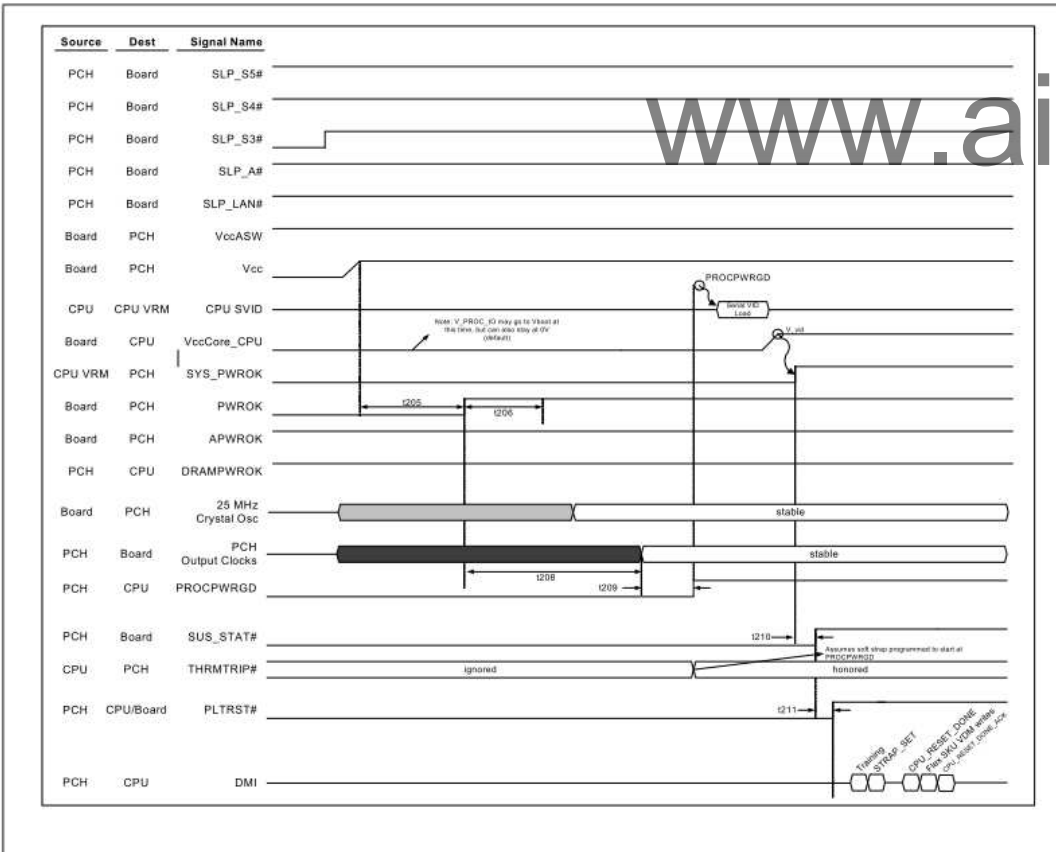


G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram



VCCSUS rail ramps up later in comparison to VCCDSW due to assumption that SLP_SUS# is used to control power to VCCSUS.

S3/M3 to S0 Timing Diagram



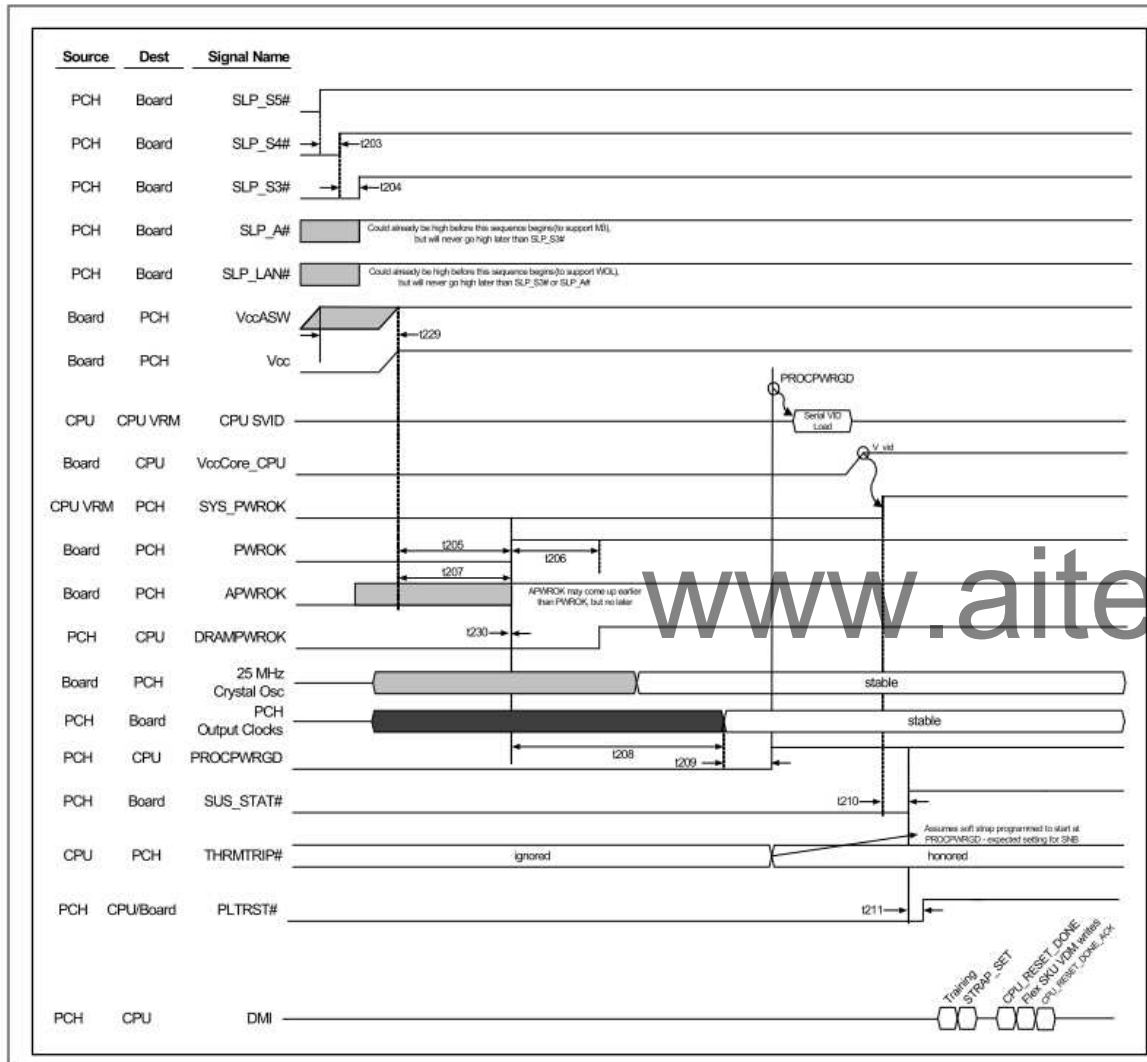
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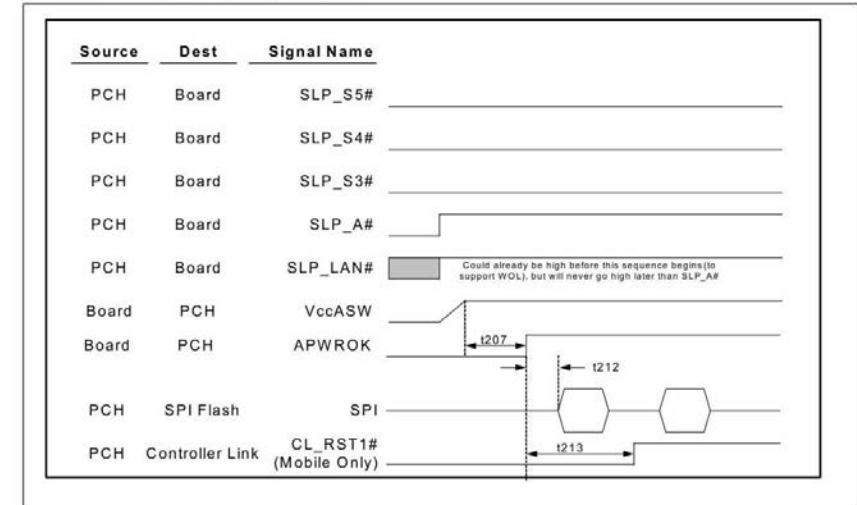
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Rev -1
vSuperb
System Power Sequence

Power Sequence

S5 to S0 Timing Diagram



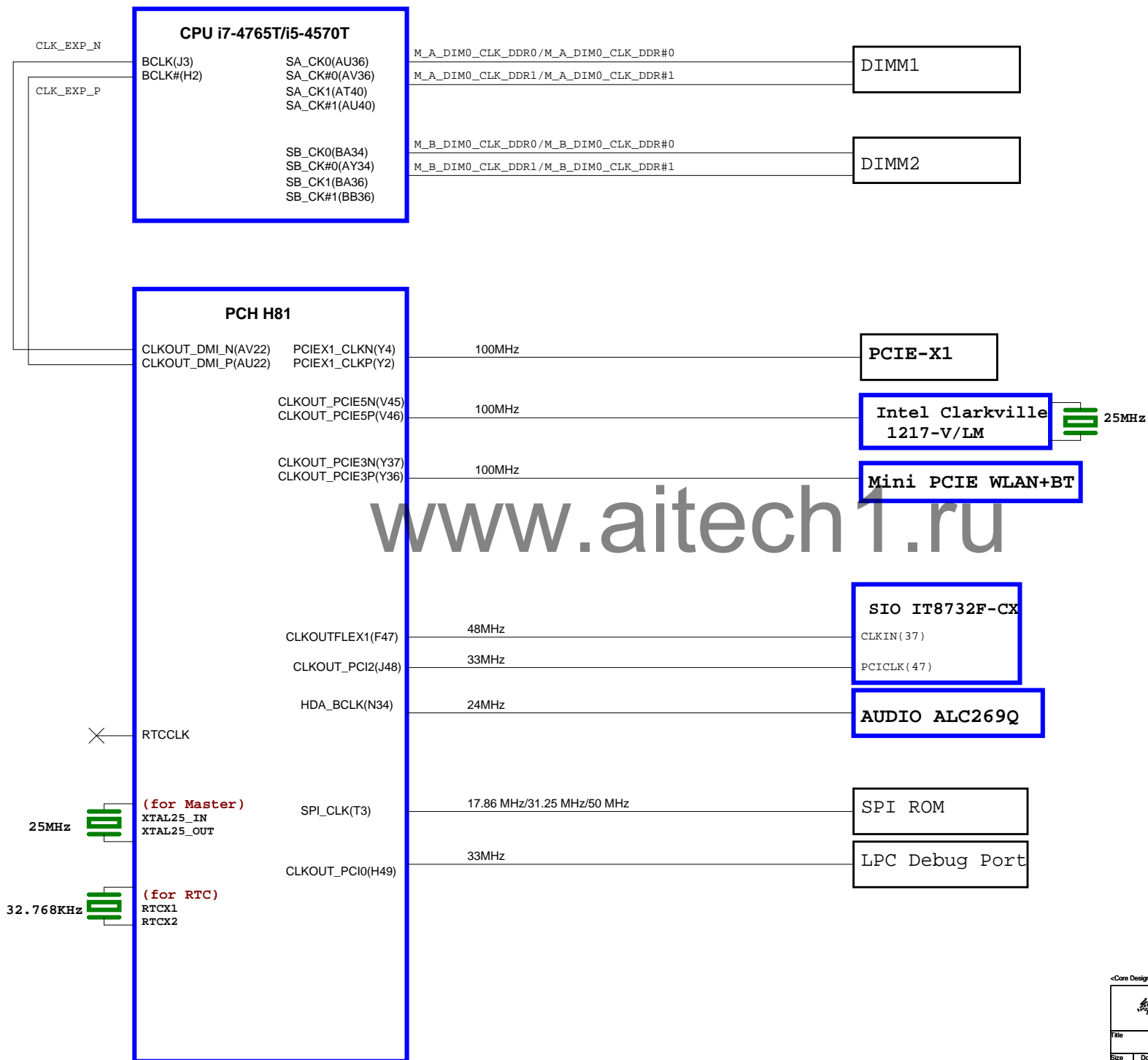
S5/Moff - S5/M3 Timing Diagram

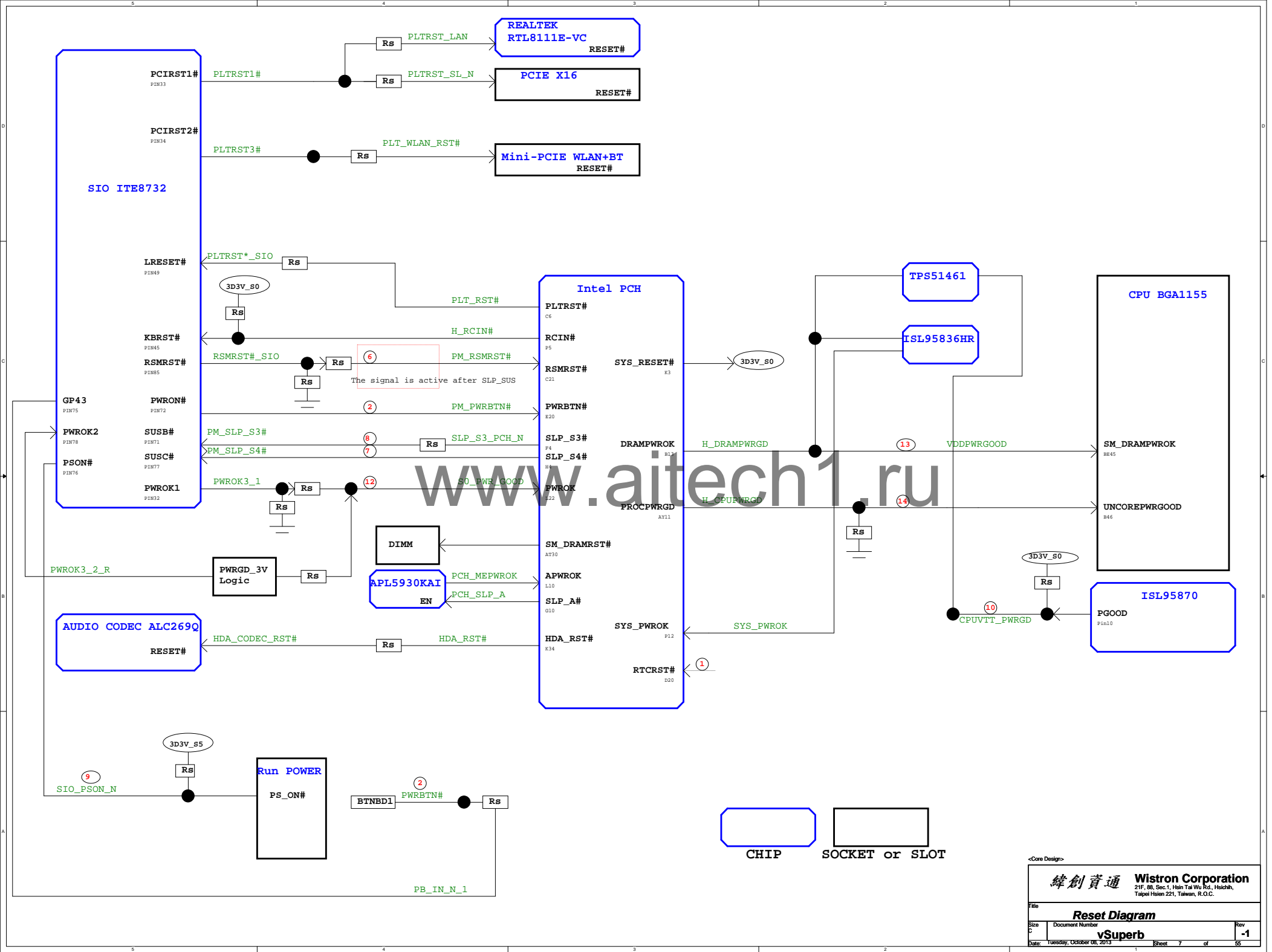


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Title
Power Sequence
Size B Document Number
vSuperb
Date: Tuesday, October 08, 2013 Sheet 5 of 55 Rev -1



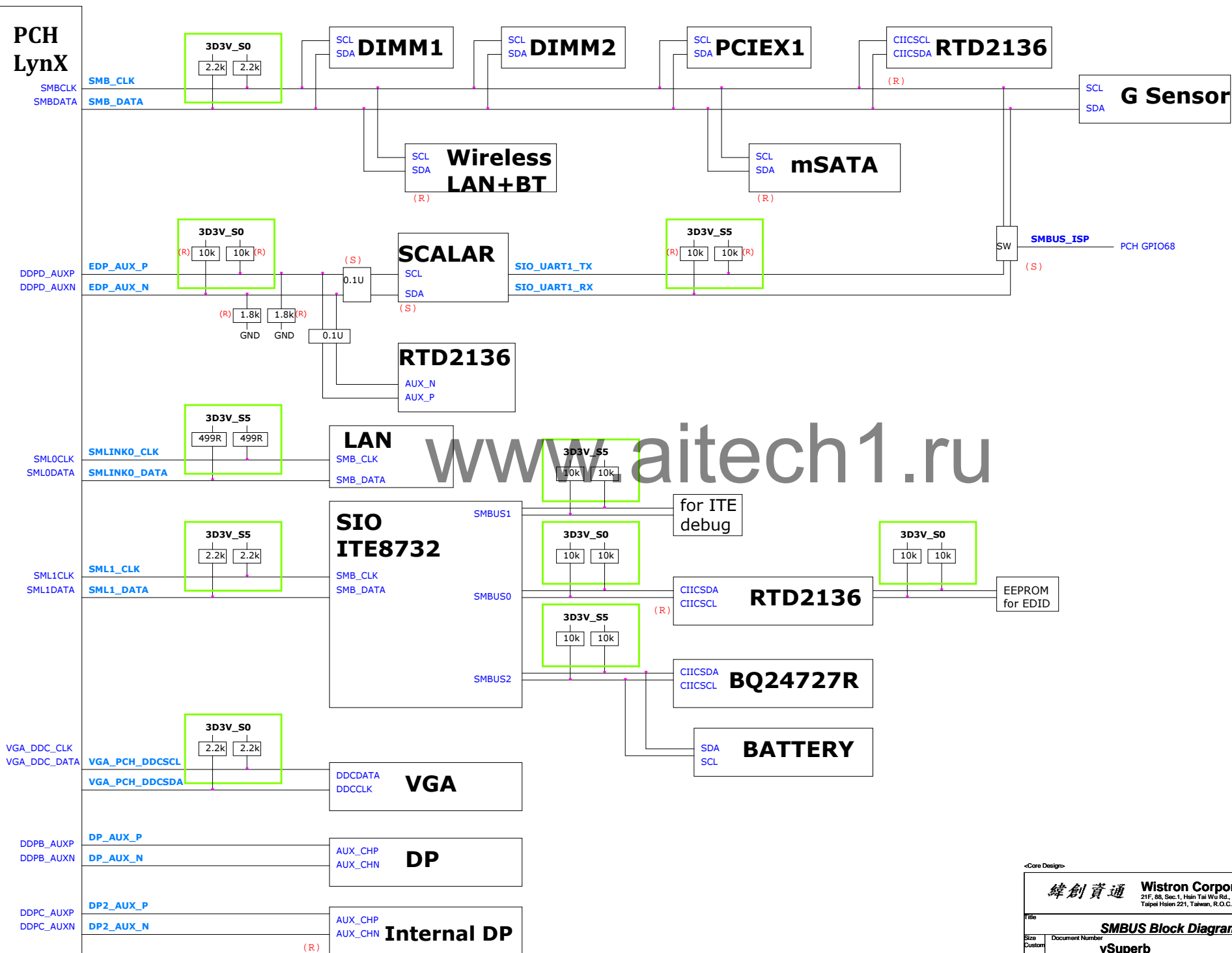


Superb GPIO Table
Version: 2013/06/03

| Item | Item Name | Default | Description | Label | Signal Name | Usage | Not Used in other data | RISC-V Programming | | | | | CS Comment / Remark | |
|--------|------------|---------|--|-----------------|--|----------------|------------------------|--------------------|--------|--------|--------|--------|--|--|
| | | | | | | | | SR | LS | US | SS | SS | | |
| GP109 | Core | GPI | Available with BMT001 only | TC_WA0 | Button input to brightness | N/A | UNCONNECTED | | GPI | GPI | GPI | GPI | Unused | |
| GP102 | Core | GPI | Multiplexed P0004 | GP202 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Pin external - 2-pin header on P0004 | |
| GP103 | Core | GPI | Multiplexed P0004 | GP203 | N/A | 100V_50 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | Pin external - 2-pin header on P0004 | |
| GP104 | Core | GPI | Multiplexed P0004 | GP204 | N/A | 100V_50 | GPIO4 | GPIO4 | GPIO4 | GPIO4 | GPIO4 | GPIO4 | Pin external - 2-pin header on P0004 | |
| GP105 | Core | GPI | Multiplexed P0004 | CS_INT0 | C-sensor interrupt | 100V_50 | GPIO | GPI | GPI | GPI | GPI | GPI | Change to GPI - Sensor output (P0004 must be used) - When using P0004, P0004 must be disabled | |
| GP108 | Core | GPI | Available as GPIO0 only | TC_A0F | ADP function | 100V_50 | GPIO | GPI | GPI | GPI | GPI | GPI | IC for P0004 for ADP function. When P0004 is used, it is not for P0004 for ADP function. | |
| GP107 | Core | GPI | Available as GPIO0 only | DB0 | Button input to enter recovery | 100V_50 | GPIO | GPI | GPI | GPI | GPI | GPI | When P0004 is used, system will do one button recovery - When P0004 is used, system will do one button recovery - When P0004 is used, system will do one button recovery | |
| GP108 | Suppl. ext | GPIO | Unimplemented | TC_IC_N | TC_IC_N | 100V_55 | Native | Native | Native | Native | Native | Native | Unimplemented, External P/N. Must not program it. | |
| GP109 | Suppl. ext | Native | Multiplexed with OC04. When configured as GPIO, default direction is input | Wake0_P0E | Wake wake event | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Pin external | |
| GP1010 | Suppl. ext | Native | Multiplexed with OC04. When configured as GPIO, default direction is input | mSATA_DET0 | mSATA detect function | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | After mSATA plug, mSATA_DET0 pin will be pulled up (P0004 must be disabled) | |
| GP1011 | Suppl. ext | Native | When configured as GPIO, default direction is input | FA0E0_INT0_EVT0 | Fixed Output0 event | 100V_55 | GPIO | GPI | GPI | GPI | GPI | GPI | When P0004 is used, system will do one button recovery - When P0004 is used, system will do one button recovery - When P0004 is used, system will do one button recovery | |
| GP1012 | D004 | Native | Multiplexed with LAN_PHY_P0E0_CTL0. P0004's Native functionality is controlled using with strap. When configured as GPIO, default direction is Output (GPIO) | LAN_P0E0A0_N | LAN Enable for P0004 (Native) P0004 Disable LAN (Native) LAN Enable LAN (Native) LAN Enable LAN (Native) | UNCONNECTED | Native | Native | Native | Native | Native | Native | Pin external | |
| GP1013 | Suppl. ext | GPI | Available as GPIO0 only | SP1_W0T_0_N | Reserved for B005 pin | 100V_4 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1014 | Suppl. ext | Native | Multiplexed with OC04. When configured as GPIO, default direction is input | Wake0_P0C_01 | POC01 wake function | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Pin external | |
| GP1015 | Suppl. ext | GPIO | Unimplemented | TLS_EN | N/A | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1016 | Core | GPI | Multiplexed with SATA00P0. Available as GPIO0 only | P0004_SP0006 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1017 | Core | GPI | Multiplexed with SATA00P0. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | P0004_SP0007 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1018 | Core | GPI | Multiplexed with SATA00P0. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | P0004_SP0008 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1019 | Core | GPI | Multiplexed with SATA00P0. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | SATA00P0 | N/A | 100V_50 | Native | Native | Native | Native | Native | Native | Unused | |
| GP1020 | Core | Native | Multiplexed with P0004B0004. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | LAN0004_INT0_N | High LAN CLK. Low LAN CLK. High LAN CLK. High LAN CLK. | UNCONNECTED | Native | Native | Native | Native | Native | Native | Unused | |
| GP1021 | Core | GPI | Multiplexed with SATA00P0 | BATT_CTL_EVT0 | High Low enter | 100V_50 | GPI | GPI | GPI | GPI | GPI | GPI | Unused | |
| GP1022 | Core | GPI | Multiplexed with S0000C0 | BOARD_D_3 | BOARD_D_3 | 100V_50 | GPI | GPI | GPI | GPI | GPI | GPI | Pin external | |
| GP1023 | Core | Native | Multiplexed with L000020 | UPC_INT02_N | N/A | 100V_50 | Native | Native | Native | Native | Native | Native | Unused | |
| GP1024 | Suppl. ext | GPIO | Unimplemented | H_SAT0002_N | High CPU mode Low Test mode | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1025 | Suppl. ext | Native | Multiplexed with P0004B0004. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | P0004_SP0009_P0 | N/A | 100V_55 to GND | Native | Native | Native | Native | Native | Native | Unused | |
| GP1026 | Suppl. ext | Native | Multiplexed with P0004B0004. External pull-up resistor required for Native function. When configured as GPIO, default direction is Output | SD0004_P0 | SD0004_P0 | 100V_55 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Pin external | |
| GP1027 | D004 | GPI | Unimplemented. An external pull-up resistor is required. When configured as GPIO, default direction is Output | LAN0004_N | LAN0004_N | 100V_55 | GPI | GPI | GPI | GPI | GPI | GPI | Unused | |
| GP1028 | Suppl. ext | GPIO | Unimplemented | STM_SEL | STM Output | 100V_4 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Pin external | |
| GP1029 | D004 | Native | Multiplexed with SUP_W0A0004 | SUP_W0A0004 | N/A | 100V_4 | Native | Native | Native | Native | Native | Native | Unused | |
| GP1030 | Suppl. ext | Native | Multiplexed with SUP_W0A0004, SUP_W0A0004 | SUP_W0A0004 | N/A | 100V_55 | Native | Native | Native | Native | Native | Native | Unused | |
| GP1031 | D004 | GPI | GPIO_004_004_004_004 Internally terminated as a pull-up, which means GPIO mode is permanently selected and cannot be changed | P0004_SP0006 | N/A | 100V_4 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1032 | Core | GPIO | Available as GPIO0 only | N/A | N/A | UNCONNECTED | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1033 | Core | GPIO | Available as GPIO0 only | SOP_ENABLE_GP03 | N/A | 100V_50 | Native | Native | Native | Native | Native | Native | Unused | |
| GP1034 | Core | GPI | Unimplemented | P0004_P04_P0 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |
| GP1035 | Core | GPIO | Available as GPIO0 only | P0004_P04_P0 | N/A | 100V_50 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | Unused | |

| | | | | | | | | | | | | |
|--------|--|--------|---|---------------------|--|------------------|--------|--------|--------|--------|--------|--|
| GPI038 | Core | GPIO | Multiplied with SATA2P0 | SATA2P0 | N/A | I/OV_30 | Native | Native | Native | Native | Native | Strapping, Reserved P/I, P/L to GND; Bios don't program it |
| GPI037 | Core | GPIO | Multiplied with SATA3GP | SATA3GP | N/A | I/OV_30 | Native | Native | Native | Native | Native | Strapping, P/I external, reserved P/L; Bios don't program it |
| GPI036 | Core | GPIO | Multiplied with SLDAD | PCH_GP38_PU | N/A | IOV30_30 | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | Unused, P/I external, 請注意 IOV30H always |
| GPI039 | Core | GPIO | Multiplied with SATA0D0 When configured as OCIE, When configured as GPIO, default direction is Input | PCH_GP39_PU | GPIO Header | IOV30_30 | GR | GR | GR | GR | GR | P/I external. |
| GPI040 | GPIO41 | | Multiplied with OCIE, When configured as GPIO, default direction is Input | USB_OC_02 | USB OC-event | IOV30_35 | Native | Native | Native | Native | Native | P/I external |
| GPI041 | | | Multiplied with OCIE, When configured as GPIO, default direction is Input | W3_DISABLE_N | High-WR-RT enable Low-WR-RT disable | IOV30_35 | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | P/I external |
| GPI042 | | | Multiplied with OCIE, When configured as GPIO, default direction is Input | W1_DISABLE_N | High-WR-RT enable Low-WR-RT disable | IOV30_35 | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | P/I external |
| GPI043 | | | Multiplied with OCIE, When configured as GPIO, default direction is Input | GPO43 | N/A | IOV30_35 | Native | Native | Native | Native | Native | Unused, P/I external |
| GPI044 | Scope end | Native | Multiplied with PCIeCLK025A. External pull-up resistor required for Native Function. When configured as GPIO, default direction is Input | USB_PWR_CLK1 | N/A | IOV30_35 | Native | Native | Native | Native | Native | Unused, P/I external |
| GPI045 | Scope end | Native | Multiplied with PCIeCLK026B. External pull-up resistor required for Native Function. When configured as GPIO, default direction is Input | PCH_GPO45 | N/A | IOV30_35 | Native | Native | Native | Native | Native | Unused, P/I external, P/L to GND |
| GPI046 | | | Multiplied with PCIeCLK027A. External pull-up resistor required for Native Function. When configured as GPIO, default direction is Input | CLK_PCIE_MLAN_REQ_# | High: Request LAN_CLK Low: N/A | IOV30_35 | Native | Native | Native | Native | Native | P/I external, P/L to GND Ps set to Native always |
| GPI040 | Clock domain controller in the package or GPIO as Native | | | INCR_GPIO040 | N/A | IOV30_30 | GR | GR | GR | GR | GR | P/I external |
| GPI048 | Core | GPIO | Multiplied with SATA0D01 | PCH_U48B_PU | GPIO Header | IOV30_30 | GR | GR | GR | GR | GR | P/I external, P/L to GND; For living up, 可以系統設置GPIO/H |
| GPI049 | Core | GPIO | Multiplied with SATA3GP | VGA_DET | Video: VGA detect Low: No VGA | IOV30_30 | GR | GR | GR | GR | GR | P/I external, P/L to GND; For living up, 可以系統設置GPIO/H |
| GPI050 | Core | GPIO | Unmultiplied | N/A | N/A | UNCONNECTED | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | Strapping, reserved P/L to GND; Bios don't program it |
| GPI051 | Core | GPIO | Unmultiplied | P_GM1_N3 | N/A | 1K P/L to GND | GPIO/H | GPIO/H | Native | Native | Native | Strapping, reserved P/L to GND; Bios don't program it |
| GPI052 | Core | GPIO | Unmultiplied | N/A | N/A | UNCONNECTED | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | Strapping, reserved P/L to GND; Bios don't program it |
| GPI053 | Core | GPIO | Unmultiplied | P_GM1_N2 | N/A | 1K P/L to GND | GPIO/H | GPIO/H | Native | Native | Native | Strapping, reserved P/L to GND; Bios don't program it |
| GPI054 | Core | GPIO | Unmultiplied | N/A | N/A | UNCONNECTED | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | Strapping, reserved P/L to GND; Bios don't program it |
| GPI055 | Core | GPIO | Unmultiplied | P_GM1_N4 | N/A | 1K P/L to GND | GPIO/H | GPIO/H | Native | Native | Native | Strapping, reserved P/L to GND; Bios don't program it |
| GPI056 | Scope end | Native | Strapping, reserved P/L to GND; Bios don't program it | Strapping-PIC26 | Warm-PIC26 | IOV30_35 | H | H | H | H | H | Strapping, reserved P/L to GND; Bios don't program it |
| GPI057 | Scope end | Native | Multiplied with SMLCLK. When configured as GPIO, default direction is Input | MEL_CLK# | Low Normal High Mode enable | IOV30_35 | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | P/I external |
| GPI058 | Scope end | Native | Multiplied with OCIE, When configured as GPIO, default direction is Input | SML_CLK# | SML_CLK | IOV30_35 | Native | Native | Native | Native | Native | P/I external |
| GPI059 | Scope end | Native | Multiplied with SMDALDET0. When configured as GPIO, default direction is Input | SRB_SLEW | RAS Control | IOV30_35 | Native | Native | Native | Native | Native | P/I external |
| GPI060 | Scope end | Native | Multiplied with SMDALDET1. When configured as GPIO, default direction is Input | MEMBST_CTRL_P0 | Memory Controller P0 | IOV30_35 | GPIO/H | GPIO/H | GPIO/L | GPIO/L | GPIO/L | P/I external |
| GPI061 | Scope end | Native | Multiplied with SMDALDET1. When configured as GPIO, default direction is Input | SUS_STAT_N | SUS_STAT_N | IOV30_35 | Native | Native | Native | Native | Native | P/I external |
| GPI062 | Scope end | Native | Multiplied with SUSCLK. When configured as GPIO, default direction is Output | SUSCLK | SUSCLK | 1K P/L to GND | Native | Native | Native | Native | Native | Unused, Reserved P/L to GND |
| GPI063 | Scope end | Native | Multiplied with SLP_SS#. When configured as GPIO, default direction is Output | SLP_SS_N | N/A | TSET POINT | Native | Native | Native | Native | Native | Unused, Tset point |
| GPI064 | Core | Native | Multiplied with CLKOUTX1EN0. When configured as GPIO, default direction is Output | N/A | N/A | UNCONNECTED | Native | Native | Native | Native | Native | Unused |
| GPI065 | Core | Native | Multiplied with CLKOUTX1N1. When configured as GPIO, default direction is Output | CLK_4BM_SIO | CLK_4BM_SIO | CONNECTED TO ESD | Native | Native | Native | Native | Native | 4BMxS Clk & SIO |
| GPI066 | Core | Native | Multiplied with CLKOUTX2EN2. When configured as GPIO, default direction is Output | N/A | N/A | UNCONNECTED | Native | Native | Native | Native | Native | |
| GPI067 | Core | Native | Multiplied with CLKOUTX1EN3. When configured as GPIO, default direction is Output | N/A | N/A | UNCONNECTED | Native | Native | Native | Native | Native | |
| GPI068 | Core | GPIO | Available as GPI068 only | SMBUS_I2P | High: Simultaneous Mode Low: I2C Slave Mode | IOV30_30 | GPIO/L | GPIO/L | GPIO/L | GPIO/L | GPIO/L | P/L, reserved P/H |
| GPI069 | Core | GPIO | Available as GPI069 only | TACHS | N/A | IOV30_30 | GPIO/L | GPIO/L | GPIO/L | GPIO/L | GPIO/L | P/L to GND, Reserved P/H, Change to GPIO/H always |
| GPI070 | Core | Native | Available as GPI070 only | KEY0_TEST | Button Test High: press key Low: Not Press key | IOV30_30 | GR | GR | GR | GR | GR | P/I external |
| GPI071 | Core | Native | Available as GPI071 only | PCH_GPD01 | N/A | IOV30_30 | Native | Native | Native | Native | Native | Unused, P/H |
| GPI072 | D5W | Native | Available as GPI072 only | USB_WAKE_SLP | USB_WAKE_SLP | IOV30_A | GPIO/L | GPIO/L | GPIO/L | GPIO/L | GPIO/L | P/I external |
| GPI073 | Scope end | Native | Multiplied with PCIeCLOCK00M. External pull-up resistor required for Native Function. When configured as GPIO, default direction is Input | PCH_GP73_P0 | N/A | 10K P/L to GND | GPIO/L | GPIO/L | GPIO/L | GPIO/L | GPIO/L | Unused, P/L to GND Change to GPIO/L always |
| GPI074 | | | Multiplied with SMLALERT/TEMP_ALERT#. When configured as GPIO, default direction is Input | SMLALERT_PCH | N/A | IOV30_35 | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H | GPIO/H |
| GPI075 | Scope end | Native | Multiplied with SML1DATA. When configured as GPIO, default direction is Input | SML1_DATA | SML1_DATA | IOV30_35 | Native | Native | Native | Native | Native | P/I external |

PCH SMBus Block Diagram



<Core Design>

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Taichung Hsien 221, Taiwan, R.O.C.

| | | | |
|--------|---------------------------|---------------------|---------|
| File | | SMBUS Block Diagram | |
| Size | Document Number | Rev | -1 |
| Custom | vSuperb | Sheet | 9 of 55 |
| Date: | Tuesday, October 08, 2013 | Sheet | 9 of 55 |

PCH Strapping

Huron River Schematic Checklist Rev.0_7

| Name | Schematics Notes |
|--|--|
| SPKR | Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-up. Leave as "No Connect". |
| GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51 | GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail. |
| SPI_MOSI | Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required. |
| NV_ALE | Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down) |
| NC_CLE | DMI termination voltage. Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN# /GPIO[33] | Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions. |
| HDA_SDO | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#. |
| GPIO15 | Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail. |
| GPIO8 | GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled. |
| GPIO27 | Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

Processor Strapping

Huron River Schematic Checklist Rev.0_7

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|----------|--|---|------------------|
| CFG[2] | PCI-Express Static Lane Reversal | 1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | 1 |
| CFG[4] | | Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: Connected to the EMBEDDED display Port | 0 |
| CFG[6:5] | PCI-Express Port Bifurcation Straps | 11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled | 11 |
| CFG[7] | PEG DEFER TRAINING | 1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training | |

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| | |
|---|--|
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| Table of Content | |
| Title Size A3 | Document Number vSuperb Date: Tuesday, October 08, 2013 |
| Rev -1 | Sheet 10 of 55 |

```

18 CK_PE_100M_MCP_DP  >>>
18 CK_PE_100M_MCP_DN  >>>

```

```

51 VCC_SENSE
51 VSS_SENSE

```

21 HSW_STRAP_13

| Signal Name | Description | Direction |
|-------------|-------------|-----------|
|-------------|-------------|-----------|

 V_{TSM}

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|-----------|---------|------------------------|-------|---------------------------|
|-----------|---------|------------------------|-------|---------------------------|

MSR_TERMINATION HSW_FCODE00[0-15] P/E reserved

伟创力 Wistron Corporation

15 M_A_DQ[0..63] <<< >>>
16 M_B_DQ[0..63]

15 M_A_DQS[0..7] <<< >>>
15 M_A_DQS#[0..7]

16 M_B_DQS[0..7] <<< >>>
16 M_B_DQS#[0..7]

| | | |
|----|--------------|---|
| 15 | M_A_A[0..15] | ↔ |
| 16 | M_B_A[0..15] | ↔ |
| | | |
| 15 | M_A_WE# | ↔ |
| 15 | M_A_CAS# | ↔ |
| 15 | M_A_RAS# | ↔ |
| 15 | M_A_BS0 | ↔ |
| 15 | M_A_BS1 | ↔ |
| 15 | M_A_BS2 | ↔ |
| | | |
| 16 | M_B_WE# | ↔ |
| 16 | M_B_CAS# | ↔ |
| 16 | M_B_RAS# | ↔ |
| 16 | M_B_BS0 | ↔ |
| 16 | M_B_BS1 | ↔ |
| 16 | M_B_BS2 | ↔ |

15 M_A_DIM0_CS#0 

15 M_A_DIM0_CS#1 

15 M_A_DIM0_CKE0 

15 M_A_DIM0_CKE1 

15 M_A_DIM0_ODT0 

15 M_A_DIM0_ODT1 

16 M_B_DIM0_CS#0 

16 M_B_DIM0_CS#1 

16 M_B_DIM0_CKE0 

16 M_B_DIM0_CKE1 

16 M_B_DIM0_ODT0 

16 M_B_DIM0_ODT1 

```

15 M_A_DIM0_CLK_DDR0
15 M_A_DIM0_CLK_DDR#0
15 M_A_DIM0_CLK_DDR1
15 M_A_DIM0_CLK_DDR#1

16 M_B_DIM0_CLK_DDR0
16 M_B_DIM0_CLK_DDR#0
16 M_B_DIM0_CLK_DDR1
16 M_B_DIM0_CLK_DDR#1

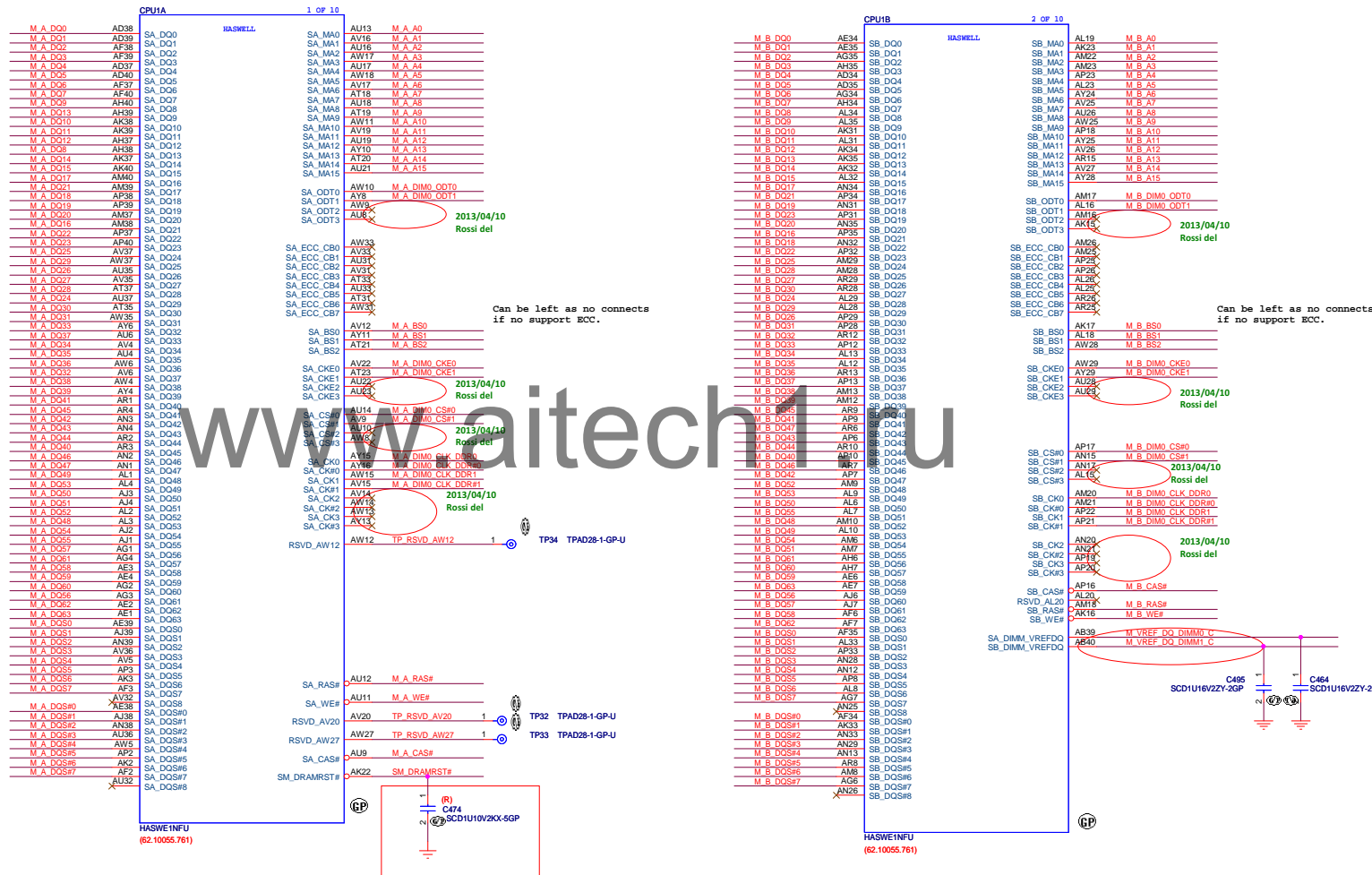
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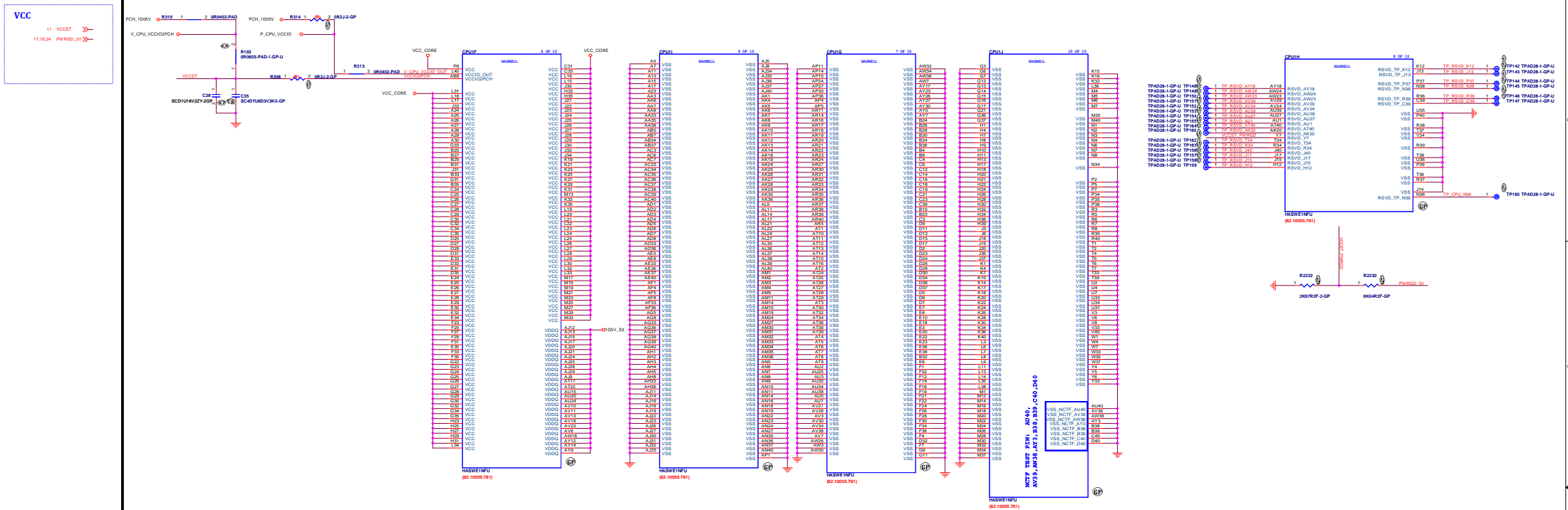
```

47 SM_DRAMRST#      <<--
47 M_VREF_DQ_DIMM1_C >>--
47 M_VREF_DQ_DIMM0_C >>--

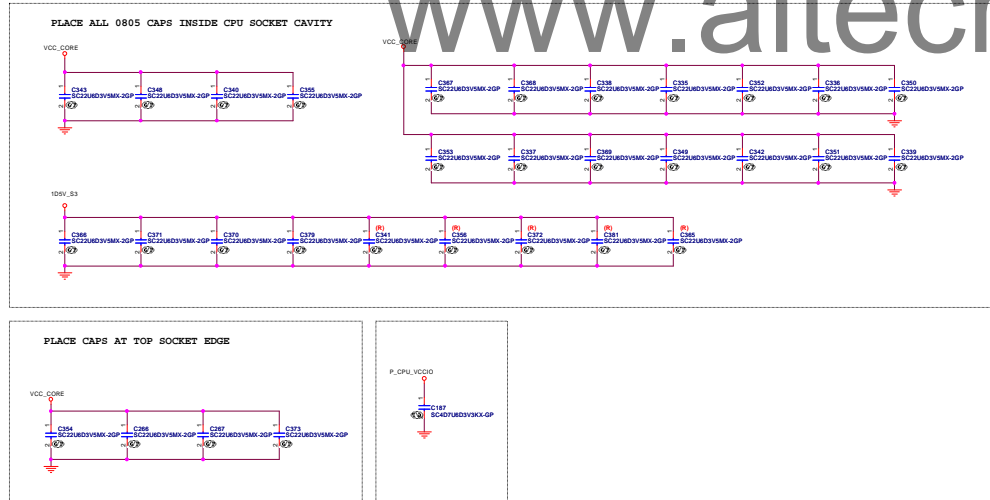
```

Rossi Change DIMM Net name reference swift





www.aitech1.ru



13 M_A_A[15:0] << >> _____

13 M_A_DQS#[7:0] << >> _____

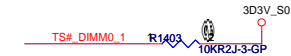
13 M_A_DQS[7:0] << >> _____

2013/05/02
Rossi Change DIMM type follow London2
Symbol--> 62.10024.B81

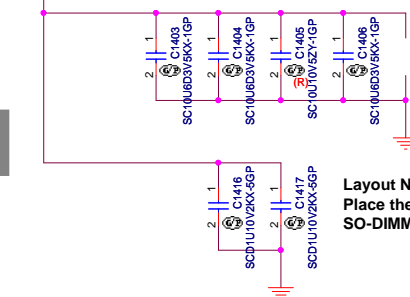
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

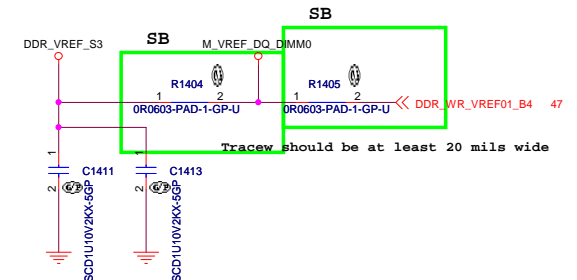
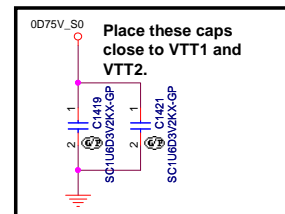
Thermal EVENT



SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA.

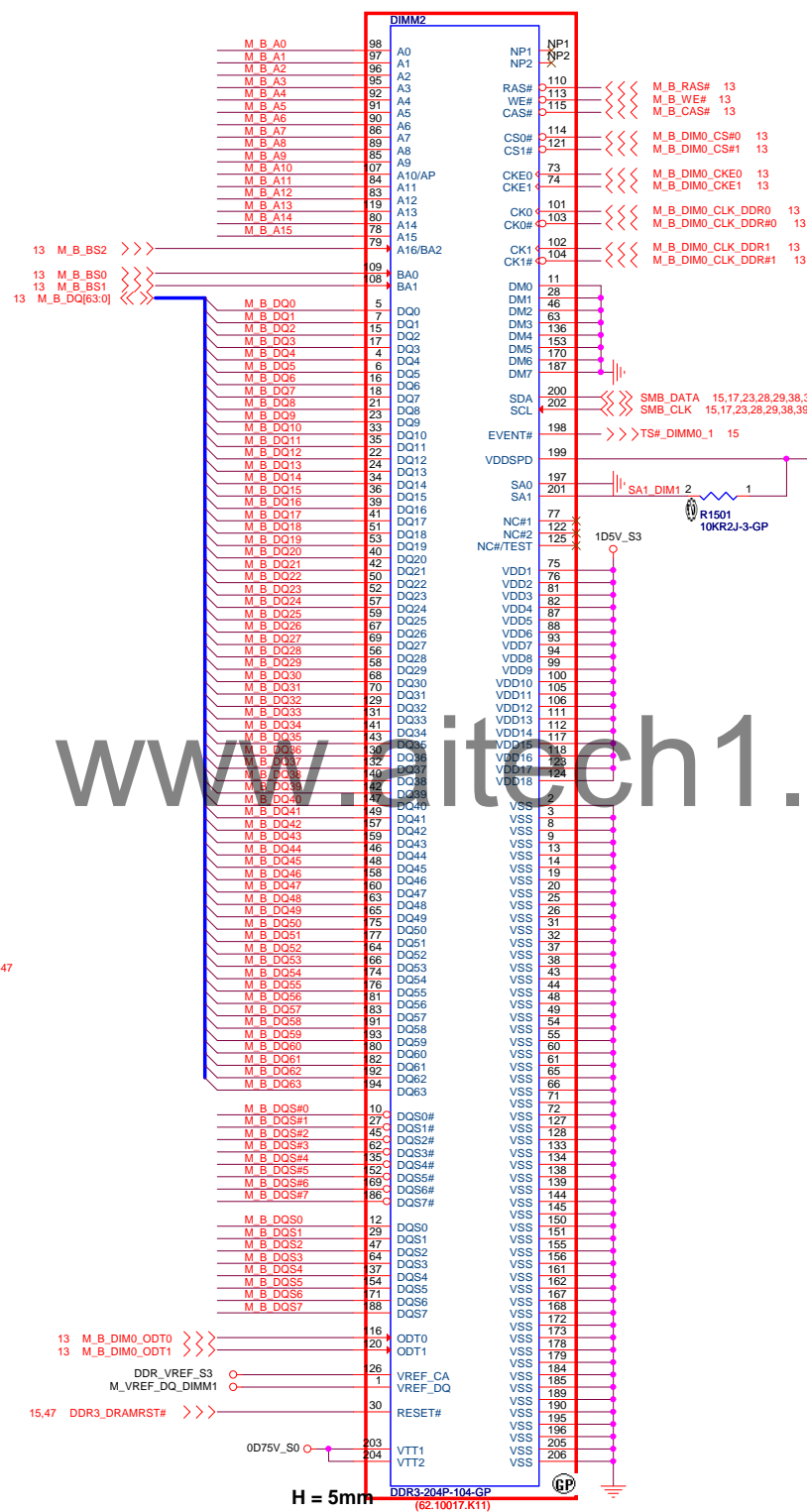
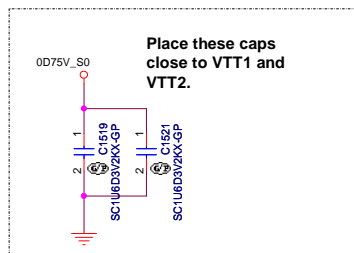
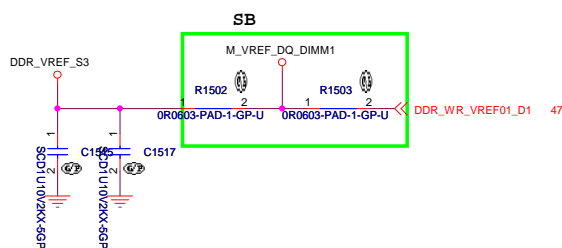
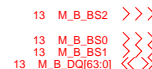
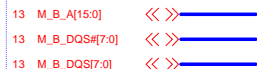


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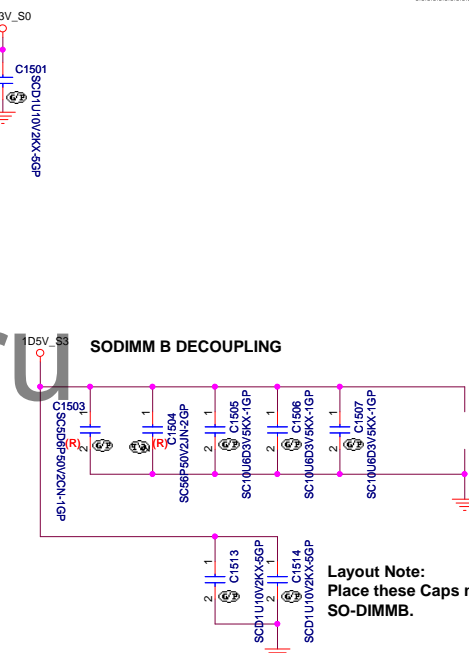
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|-------------------|---------------------------|-------------|-----------|
| Title | | | |
| DDR3-DIMM1 | | | |
| Size Custom | Document Number | | Rev |
| | vSuperb | | -1 |
| Date: | Tuesday, October 08, 2013 | Sheet 15 of | 55 |

H = 8mm
DDR3-204P-101-GP-U
(62.10017.K01)

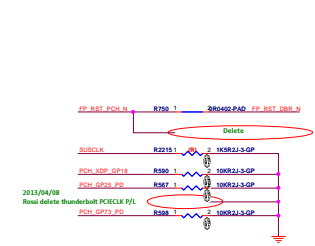
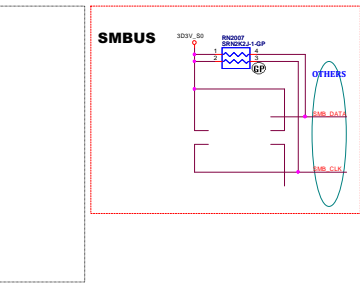
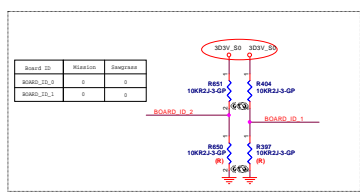
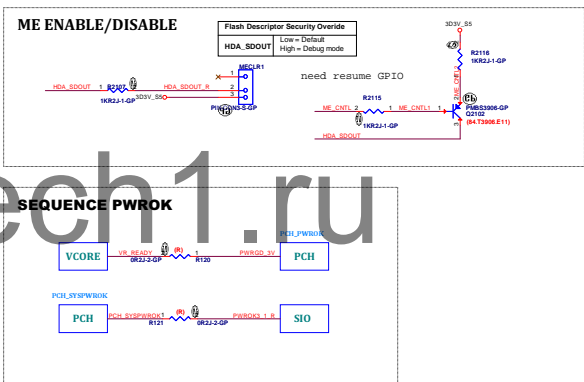
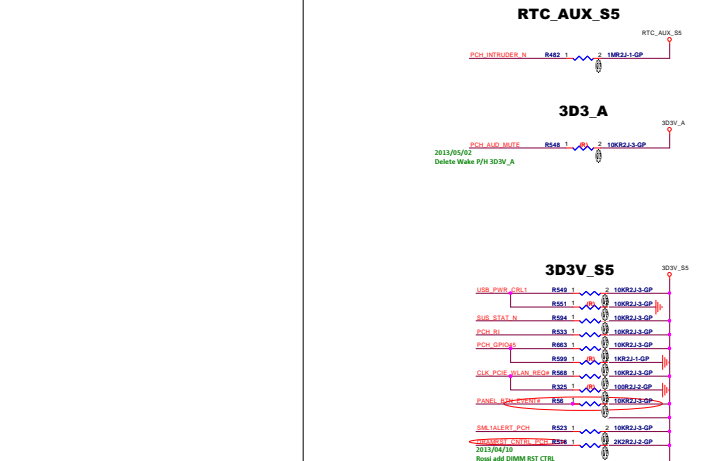
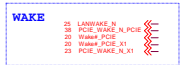


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near
SO-DIMMB.



PCI CLOCK

44 CLK_PCI_LPC
20 CK_PCH_33M_FB
24 CLK_PCI_SIO

PCIE CLOCK

11 CK_DPNS_R_DN
11 CK_DPNS_R_DP
11 CK_PE_100M_MCP_DN
11 CK_PE_100M_MCP_DP
12 CK_DP_DN
12 CK_DP_DP

23 PCIE1_CLKP
23 PCIE1_CLKN
25 CK_PCIE_3_GLAN_DN
25 CK_PCIE_3_GLAN_DP
38 CLK_PCIE_WLAN
38 CLK_PCIE_WLAN#

48M CLOCK

24 CLK_48M_SIO

Rossi add for EMI

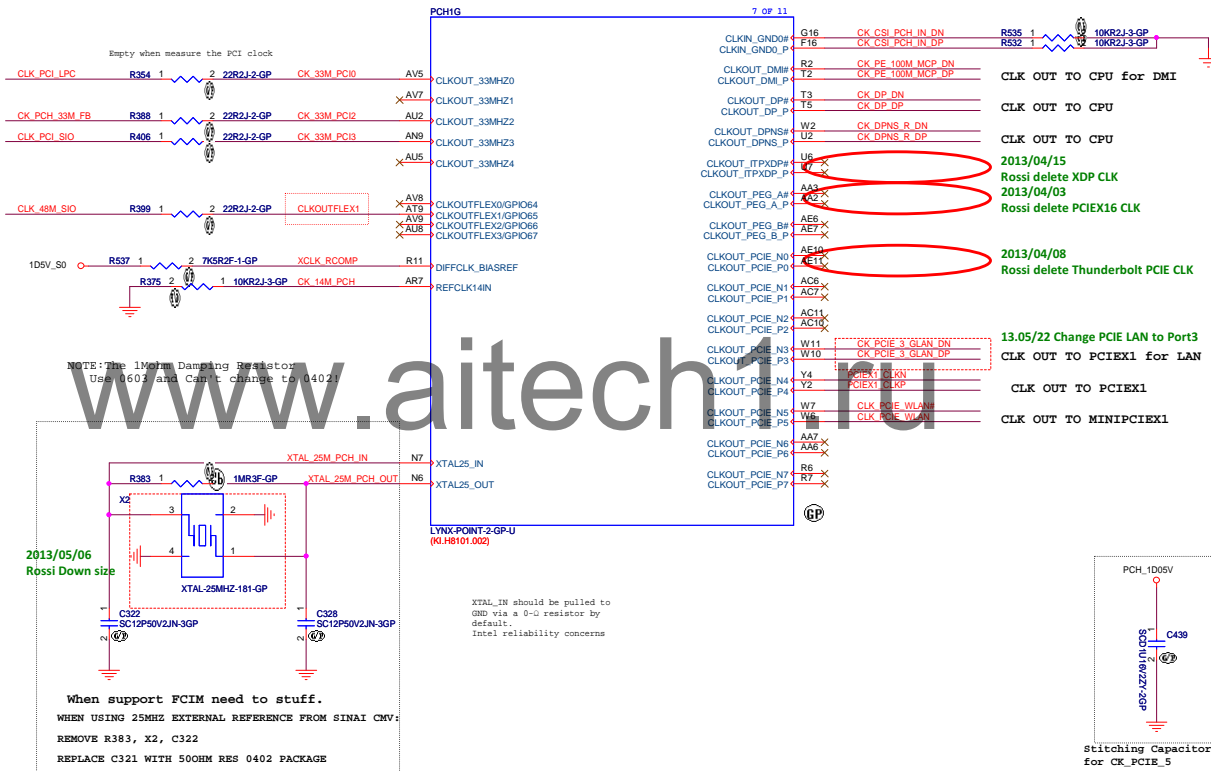


To LPC/TPM

LOOPBACK CLK

To SIO

To SIO

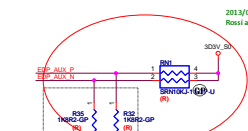
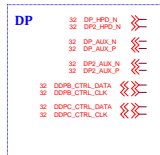


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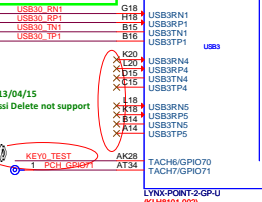
| Title | | | |
|-----------|---------------------------|-------|----------|
| PCH Clock | | | |
| Size | Document Number | Rev | |
| C | vSuperb | -1 | |
| Date: | Tuesday, October 08, 2013 | Sheet | 18 of 55 |



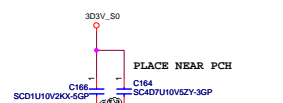
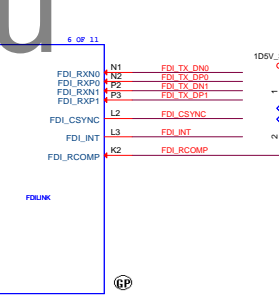
NOTES:

1. Contact your local Intel Field Sales Representative for currently available PCI SKUs.
2. Table 1-3 shows feature differences between the Intel SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCI-to-PeP Bridge. See Section 5.3 for more details.
4. The number of PCI Express ports available depends on the Flexible I/O configuration. See Section 2.7 and Table 1-3.
5. USB 2.0 ports 6 and 7 are disabled on 12 port SKUs.
6. USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
7. USB 3.0 ports 1 and 2 requires High Speed I/O ports 5 and 6 to be configured as USB 3.0. See Section 2.7 and Table 1-3.
8. Only USB 3.0 ports 1 and 2 are enabled.
9. When Flexible I/O ports are configured as USB 3.0, the total number of USB 2.0 only ports reduces in direct proportion.
10. 6 SATA ports requires High Speed I/O ports 13 and 14 to be configured as SATA. See Section 2.7 and Table 1-3.
11. SATA ports 2 and 3 are disabled on 4 port SKUs.
12. SATA 6 Gb/s support on ports 0,1,2 and 3. SATA ports 0,1,2 and 3 also support 3 Gb/s and 1.5 Gb/s.
13. SATA 6 Gb/s support on ports 0 and 1 only. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
14. Intel® Smart Response Technology requires Intel® Core™ processor.
15. Intel® Smart Response Technology requires an Intel® Core™ processor.
16. Intel® Small Business Advantage requires an Intel® Core™ processor.
17. Intel® Small Business Advantage with the Intel® H87 Express Chipset requires SMB firmware.
18. Intel® Rapid Start Technology requires an Intel® Core™ processor.
19. Intel® Identity Protection Technology requires an Intel® Core™ processor.
20. Near Field Communication is only supported in All-In-One system designs.

OTHERS

[illegible]

OC[0..3] for Ports 0-7
OC[4..7] for Ports 8-13



◀Core Design▶

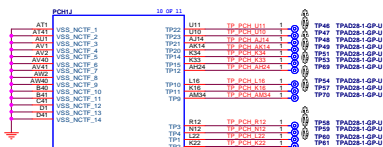
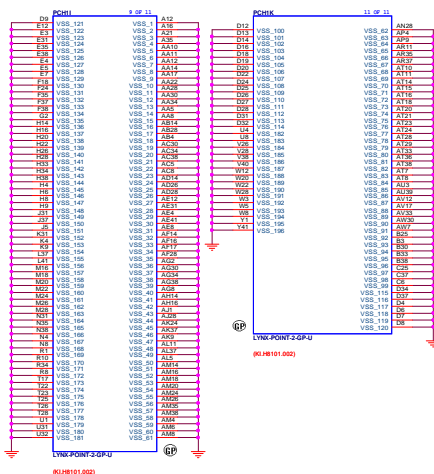
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| | | | |
|------------------------------|---------------------------|-----------|----------|
| Title | | | |
| PCH(FDI/PCIE/DMI/USB) | | | |
| Size | Document Number | Rev | |
| Custom | vSuperb | -1 | |
| Date: | Tuesday, October 08, 2013 | Sheet | 20 of 55 |

FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORT5
SOFT STRAP TO DETERMINE NATIVE FUNCTION

STRAP

| | | |
|-----|--------------|--|
| 11 | NEW_STRAP_13 | |
| 12 | SATA2SP | |
| 13 | SATA2GP | |
| 14 | RTC_AUX_S5 | |
| 15 | HDA_SDO | |
| 16 | DOVRMEN | |
| 17 | DOVRMEN | |
| 18 | DOVRMEN | |
| 19 | DOVRMEN | |
| 20 | DOVRMEN | |
| 21 | DOVRMEN | |
| 22 | DOVRMEN | |
| 23 | DOVRMEN | |
| 24 | DOVRMEN | |
| 25 | DOVRMEN | |
| 26 | DOVRMEN | |
| 27 | DOVRMEN | |
| 28 | DOVRMEN | |
| 29 | DOVRMEN | |
| 30 | DOVRMEN | |
| 31 | DOVRMEN | |
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| 33 | DOVRMEN | |
| 34 | DOVRMEN | |
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| 98 | DOVRMEN | |
| 99 | DOVRMEN | |
| 100 | DOVRMEN | |



LNK POINT 2 GPU

LNK POINT 2 GPU

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30V_S5

30V_S5

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30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

30V_S5

BOOT SELECT STRAPS

| BOOT DEVICE | GP1 / GP101 | SATA2GP / GP1019 |
|-------------|-------------|------------------|
| LPC | 0 | 0 |
| SPI | 1 | 1 |

DESIGN NOTE:
WEAK INTERNAL PULLUP ON GP51. DEFAULT SPI BOOT DEVICE

DESIGN NOTE:
ONE DE TERMINATION

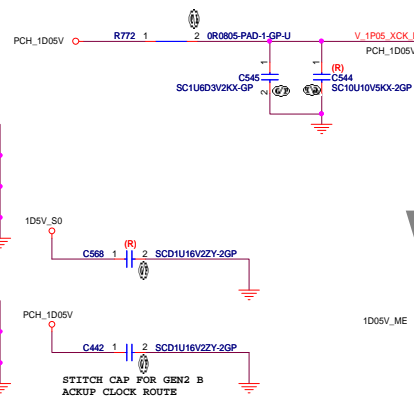
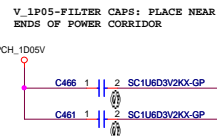
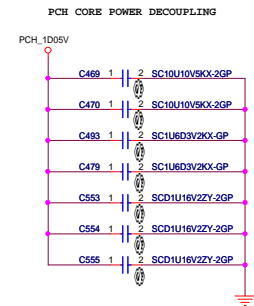
DESIGN NOTE:
LOW/HS CIPHER SUITE WITH NO CONFIDENTIALITY.

DESIGN NOTE:
HIGH/LS CIPHER SUITE WITH CONFIDENTIALITY.

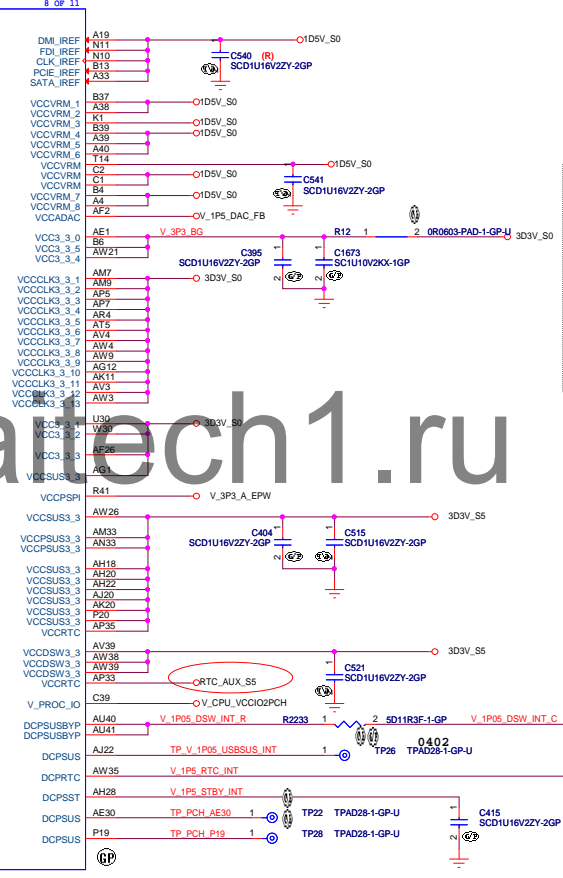
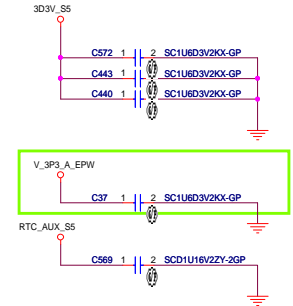
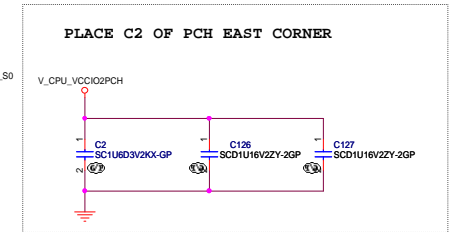
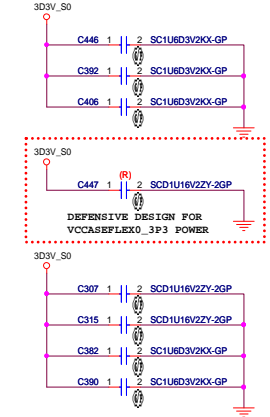
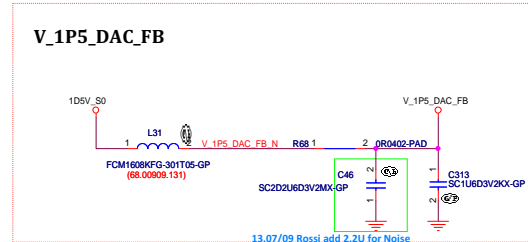
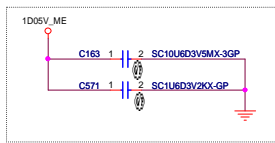
| | |
|---------------------------------|-------------------|
| DOVRMEN - On Die DOVRMEN Enable | |
| DOVRMEN | Enabled (DEFAULT) |
| DOVRMEN | Disabled |

HASWELL Straps





STITCH CAP FOR GRN2 B
ACKUP CLOCK ROUTE



www.aitech1.ru

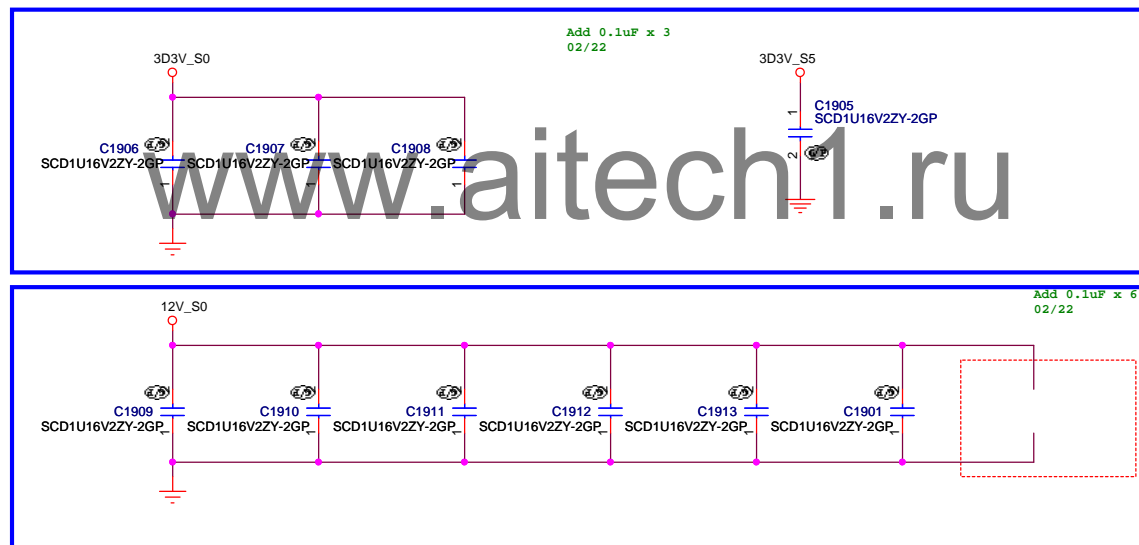
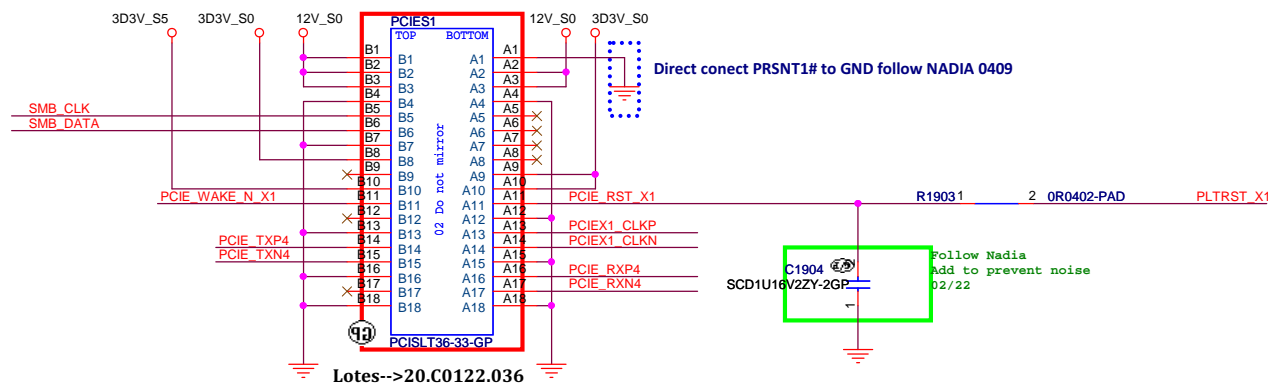
(KL.H8101.002)

| | | | |
|-----------|-----------------------|--------|---|
| INTVIRMEN | Integrated VRM Enable | Always | <p>This signal does not have an internal resistor; an external resistor is required.</p> <p>0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VRM powering option is for Mobile Only. Other systems should not pull the strap low.</p> <p>1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating.</p> <p>NOTES:</p> <ol style="list-style-type: none"> This signal is always sampled. This signal is in the RTC well. |
|-----------|-----------------------|--------|---|

PCIE

15,16,17,28,29,38,39,41 SMB_CLK
15,16,17,28,29,38,39,41 SMB_DATA
20 PCIE_TXP4
20 PCIE_TXN4
18 PCIE_X1_CLKP
18 PCIE_X1_CLKN
20 PCIE_RXP4
20 PCIE_RXN4
17 PCIE_WAKE_N_X1
24 PLTRST_X1

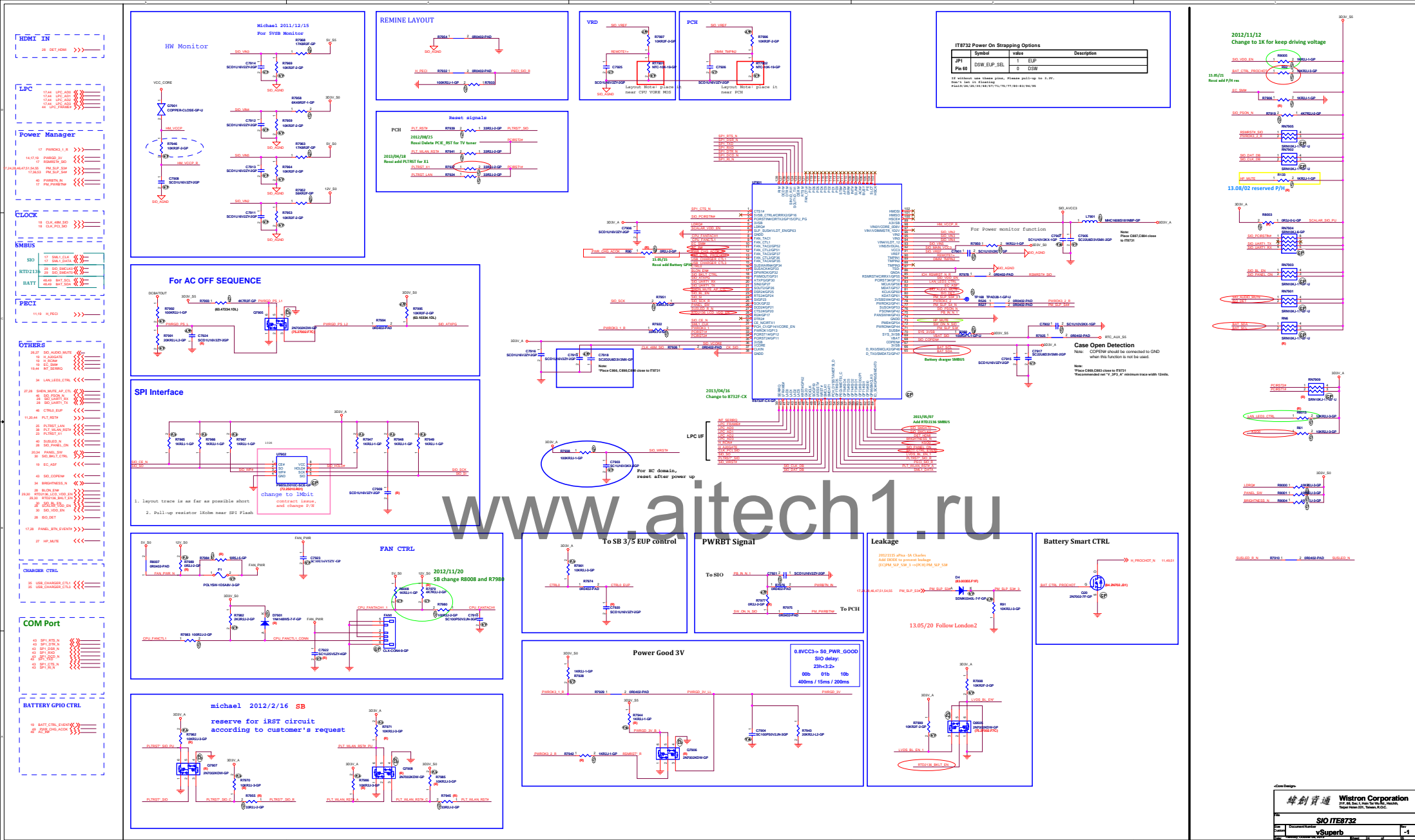
PCIEX1 CONN



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---------------------------------|-----------------|-----|
| Title | | |
| PCIEX1 | | |
| Size B | Document Number | Rev |
| vSuperb | | -1 |
| Date: Tuesday, October 08, 2013 | Sheet 23 of 55 | |




```

17 AUD_LINK_SDIN
17 HDA_CODEC_SDOUT
17,27 HDA_CODEC_RST#
17 HDA_CODEC_SYNC
17 HDA_CODEC_BITCLK

```

```

37 DMIC_DATA
37 DMIC_CLK

```

| | | |
|----|-------------|----|
| 27 | SPEAKER1_L1 | ≡≡ |
| 27 | SPEAKER1_R1 | ≡≡ |
| | | |
| 27 | FM_R_CODEC | ≡≡ |
| 27 | FM_L_CODEC | ≡≡ |
| | | |
| 27 | MIC2_R | ≡≡ |
| 27 | MIC2_L | ≡≡ |
| 27 | MIC2_VREF0 | ≡≡ |
| | | |
| 27 | LINE1_R | ≡≡ |
| 27 | LINE1_L | ≡≡ |
| 27 | COMBO JACK | ≡≡ |
| | | |
| 34 | MIC_IN_JD | ≡≡ |
| 27 | JD_HP_R | ≡≡ |
| 27 | JD_LOT_R | ≡≡ |
| | | |
| 27 | F_HPO_R | ≡≡ |
| 27 | F_HPO_L | ≡≡ |
| 27 | MIC0PREF | ≡≡ |

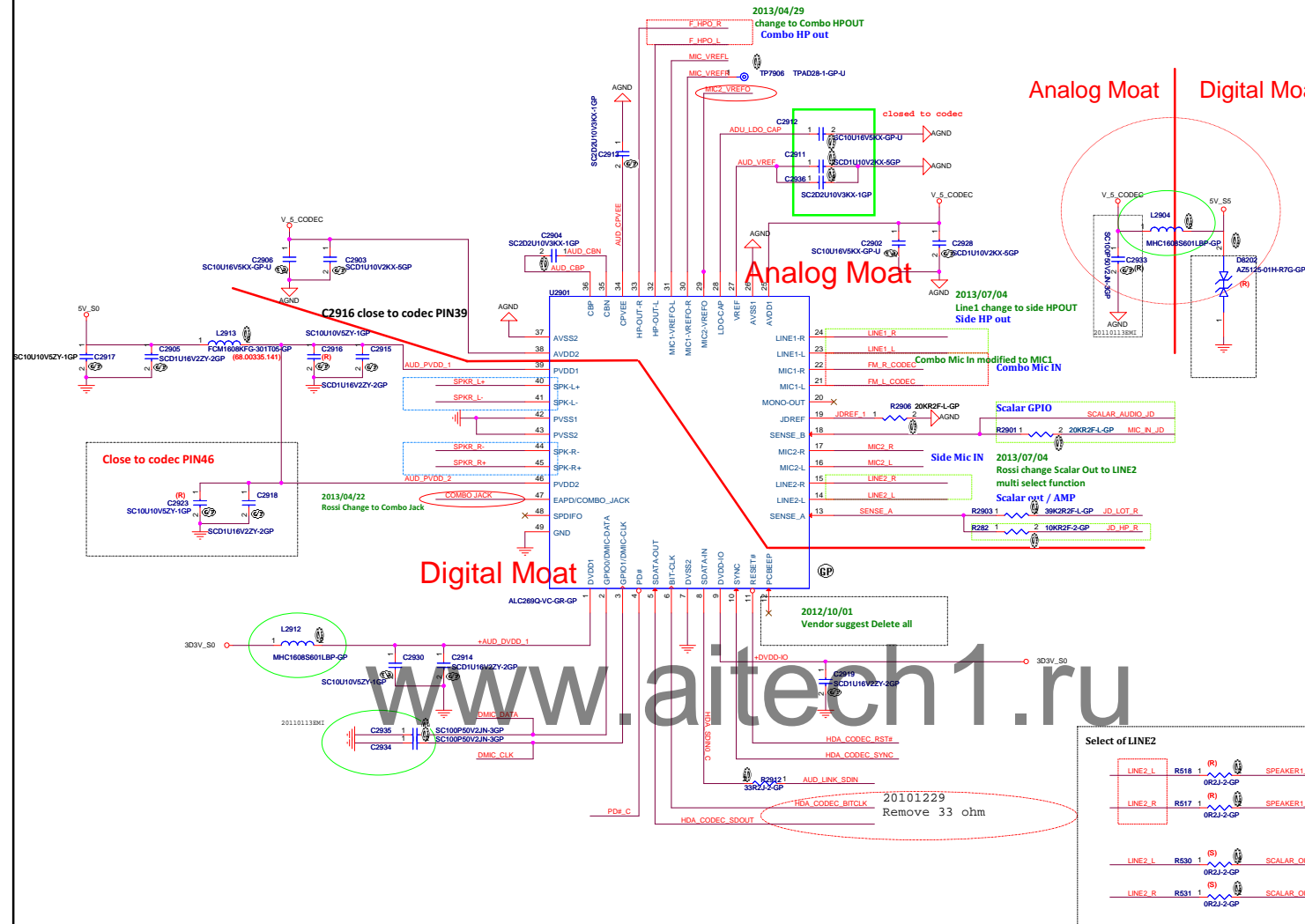
```

28 SCALAR_SENSE_B
28 SCALAR_OUT_R
28 SCALAR_OUT_L

```

27 SPKR_L+ —
27 SPKR_L- —
27 SPKR_R- —
27 SPKR_R+ —

24,27 SIO_AUDIO_MUTE >>—



303V_S5

R1106 1KR2J-1-GP (N)

R1107 1KR2J-1-GP (N)

R1109 10KR2J-3-GP (N)

R525 0R2J-2-GP (R)

Q297 P4MB3304-1-GP (N84.T3904.K11)

Q298 P4MB3304-1-GP (N84.T3904.K11)

HDA_CODEC_RST#

AUD_LNK_RST_N#1

PD_N1

PD_C

SIO_AUDIO_MUTE#1

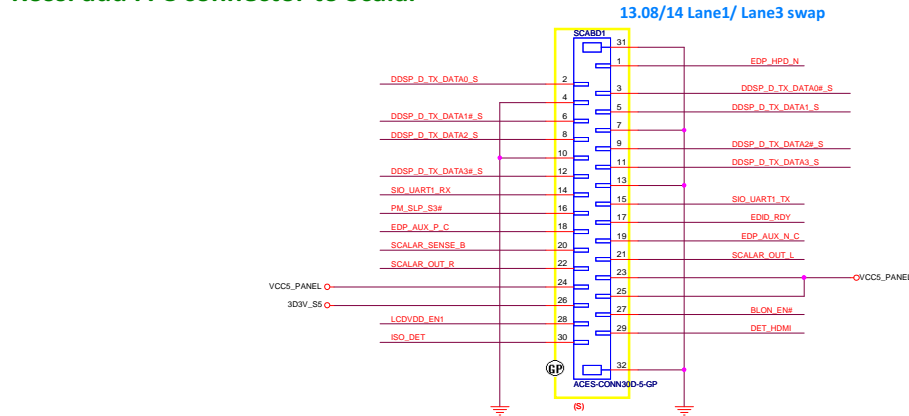
SIO_AUDIO_MUTE#2

Mount if exist AM

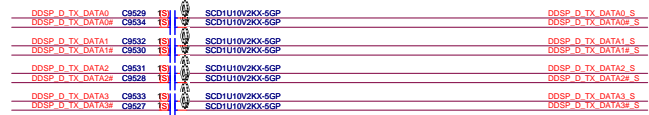
2013/04/23
Change to SIO Control

Timing diagram for the 74VHC163 4-bit counter. The diagram shows the relationship between the clock (CLK), enable inputs (EN1, EN2), and the four outputs (Q0, Q1, Q2, Q3). The clock is a square wave. EN1 and EN2 are active-low inputs. Q0, Q1, Q2, and Q3 are the counter outputs. The diagram shows the counter counting from 0 to 15. The outputs are labeled with their binary values and the corresponding decimal value in parentheses. The clock period is 10 ns. The output Q0 has a maximum delay of 10 ns. The output Q1 has a maximum delay of 10 ns. The output Q2 has a maximum delay of 10 ns. The output Q3 has a maximum delay of 10 ns.

2012/09/17
Rossi add FFC connector to Scalar



eDP



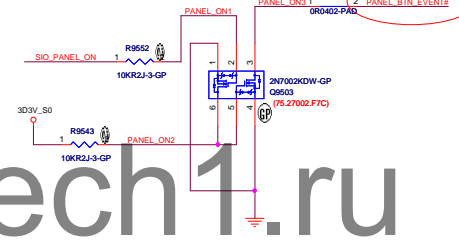
Rework C9529~C9645 if verify scalar function

2013/04/15

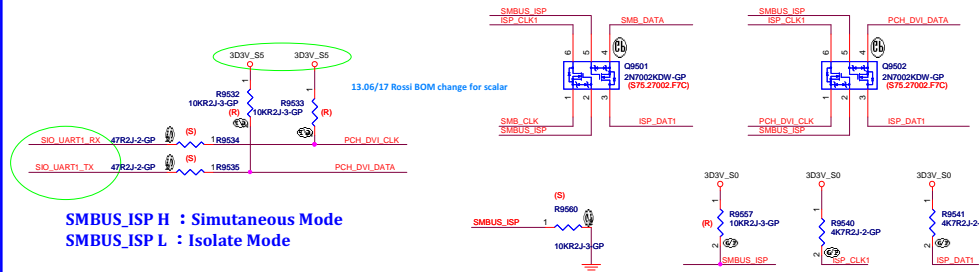
Delete redundant P/H



Panel ON/OFF



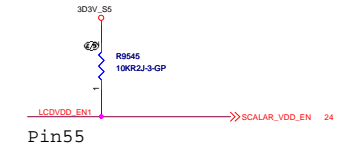
Firmware update by SMBUS



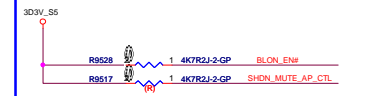
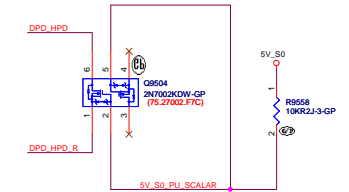
SMBUS_ISP H : Simultaneous Mode
SMBUS_ISP L : Isolate Mode

LCD ON/OFF

Michael 2011/12/02
Need check the Panel power later



Michael 2012/3/15 1A
for leakage





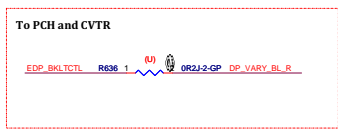
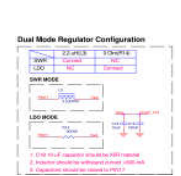
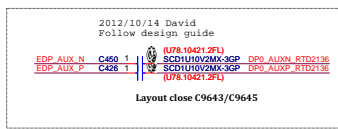
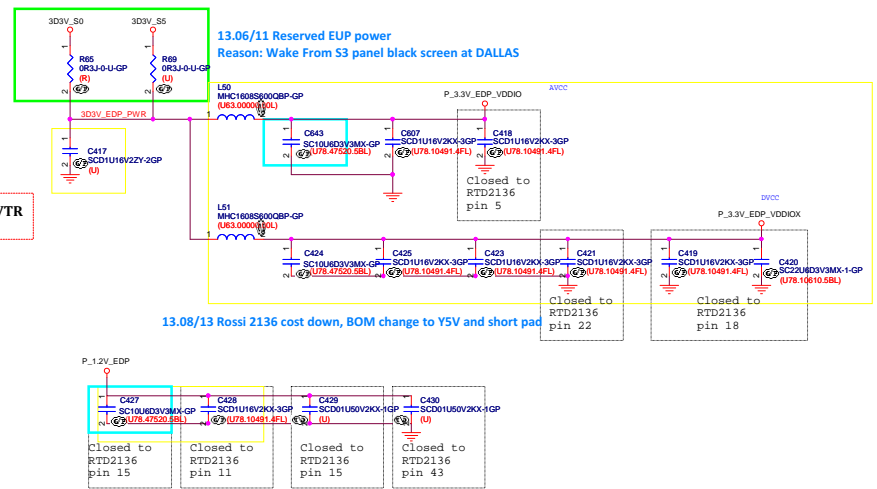
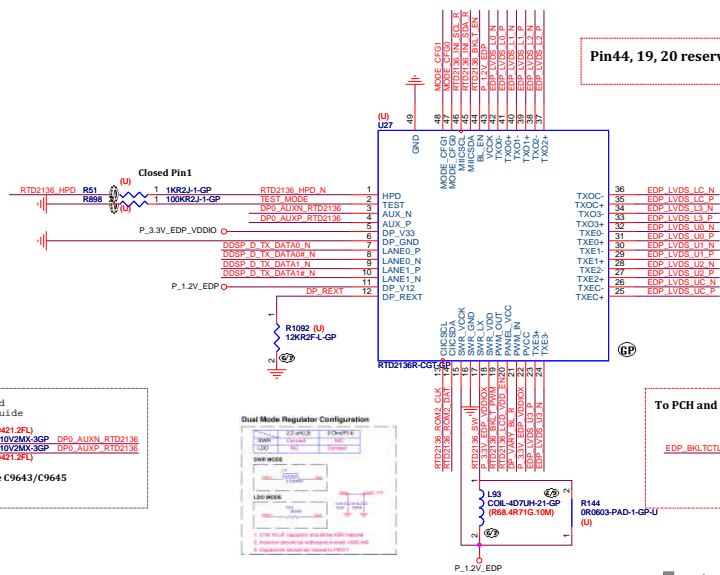
eDP to dual channel LVDS

2012/11/07

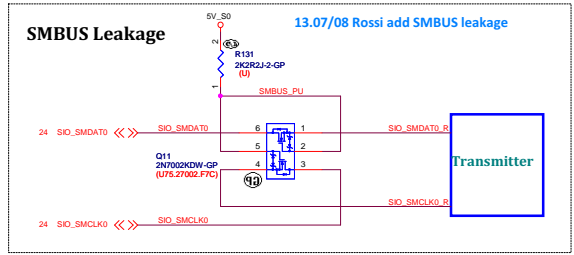
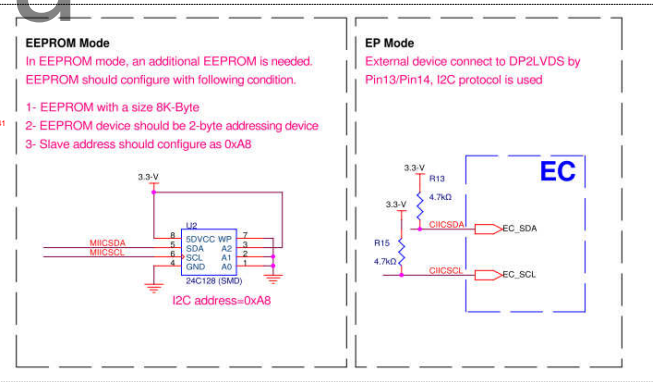
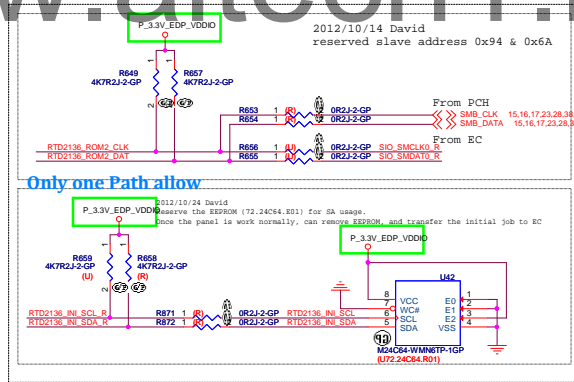
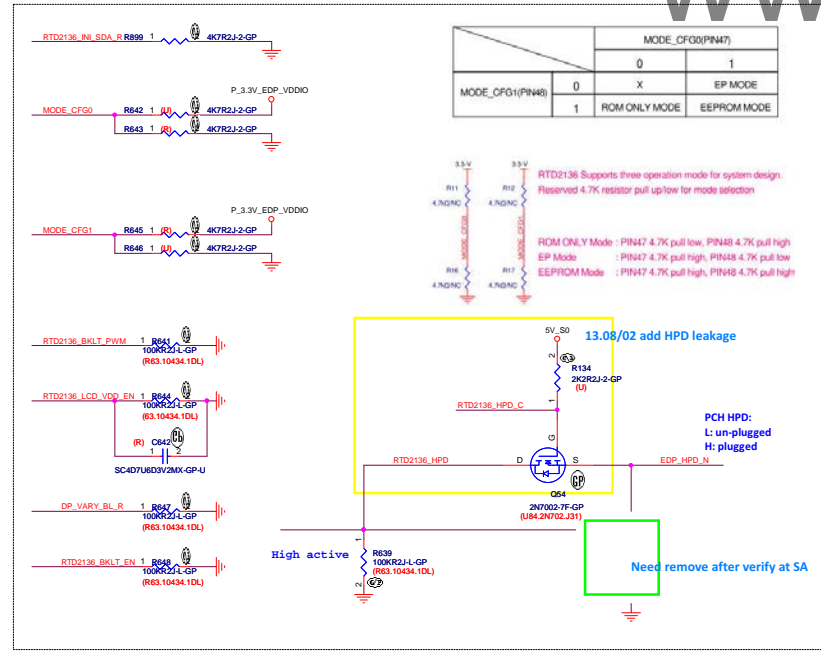
Change from PS8625 to RTD2136R Kenyon

Copy from ROSA PBAIO

RTK RTD2136R/71.02136.B03



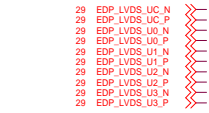
www.aitech1.ru



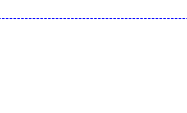
```

29 EDP_LVDS_LC_N
29 EDP_LVDS_LC_P
29 EDP_LVDS_L0_N
29 EDP_LVDS_L0_P
29 EDP_LVDS_L1_N
29 EDP_LVDS_L1_P
29 EDP_LVDS_L2_N
29 EDP_LVDS_L2_P
29 EDP_LVDS_L3_N
29 EDP_LVDS_L3_P

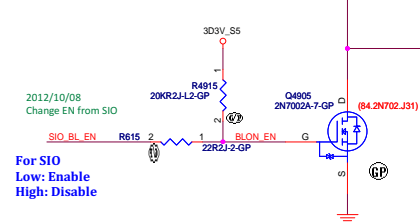
```



| | | | |
|-------|-------|--------------------|--|
| | 24 | SIO_BLEN | |
| | 19 | EDP_BKLTEN | |
| 24,29 | | RTD2136_BKLT_EN | |
| | | | |
| | 24 | SIO_BKLT_CTRL | |
| | 19,29 | EDP_BKLTCT | |
| 29 | | RTD2136_BKLT_PWM | |
| | | | |
| | 19 | EDP_VDDEN | |
| | 24 | SIO_VDD_EN | |
| 24,29 | | RTD2136_LCD_VDD_EN | |

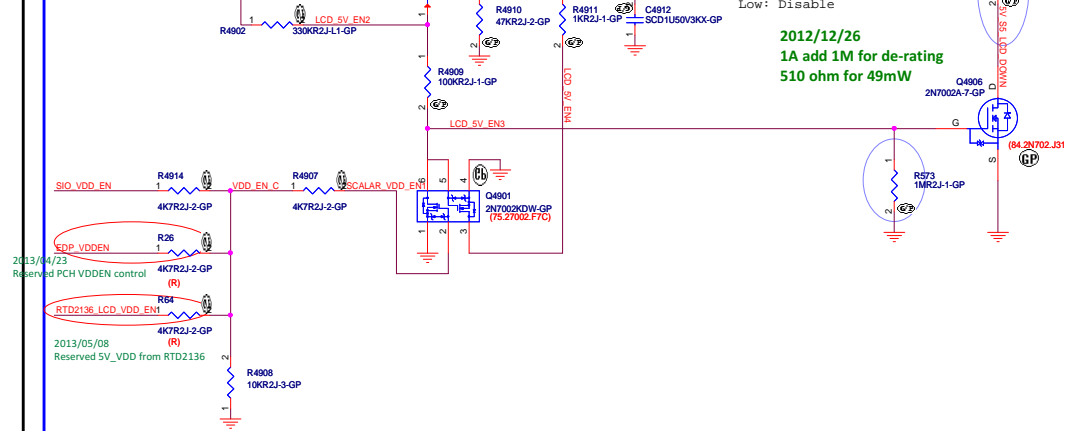
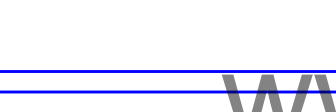


2013/05/08
Reserved EN from RTD2136



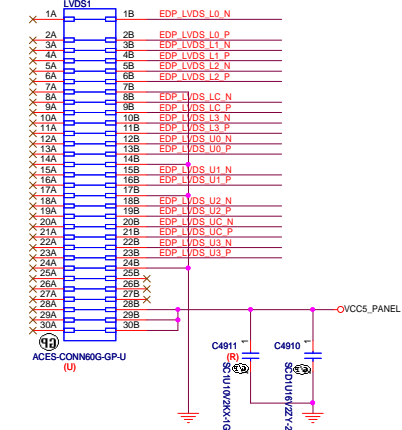
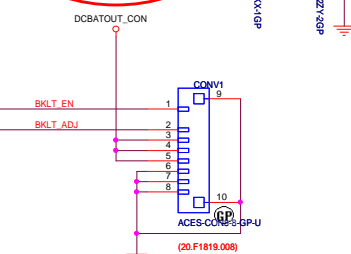
2013/04/24
Reserved PWM from PCH
EDP_BKLTCTL 2 1 100R2J-2-GP

2013/05/08
Reserved PWM from RTD2136
RTD2136_BKLT_PWM 2 1 100R2J-2-GP

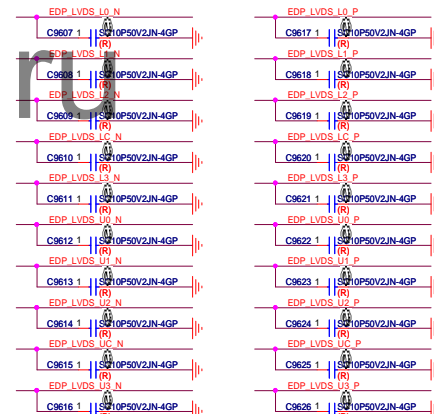


+19V_S5_INV Power
68.00216.191
Z=80 ohm,Rdc=0.02 ohm
I=5A ,0805

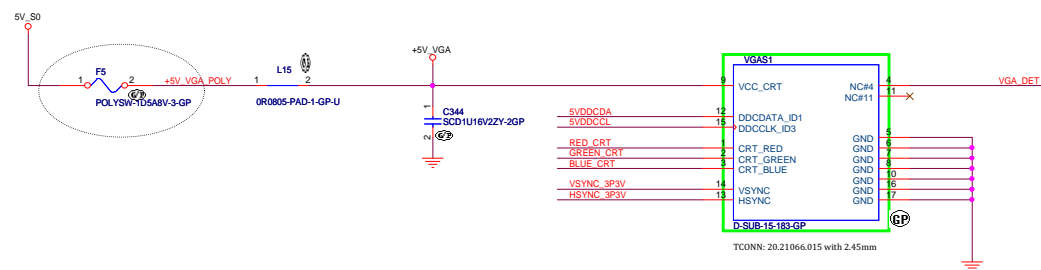
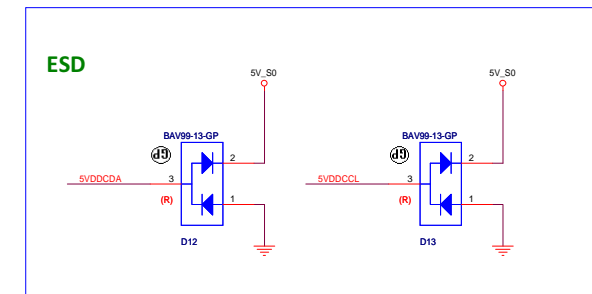
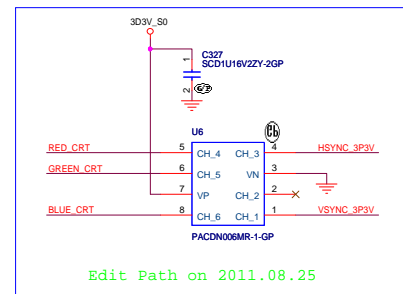
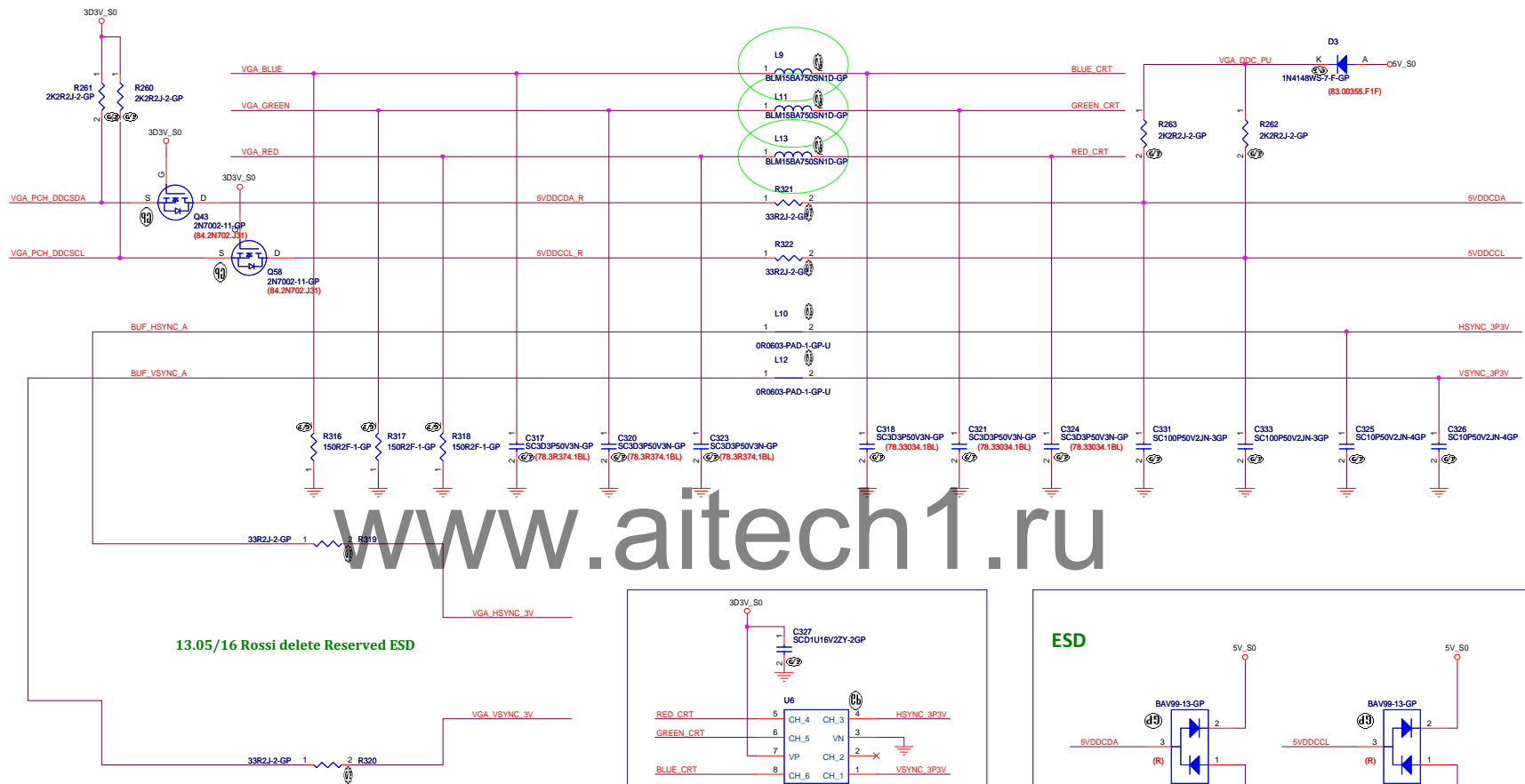
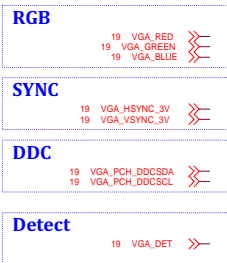
1 F4 2 DCBAT01T CON
POLYSW-1DS24V-GF
2 F3 2
POLYSW-1DS24V-GF
(R)
C280 1
C281 1
19V

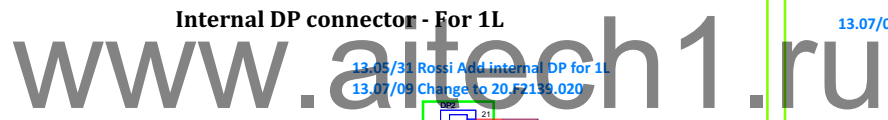
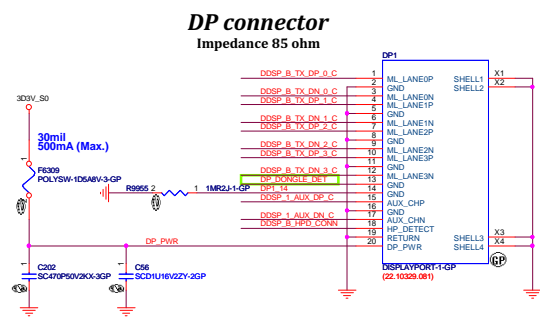
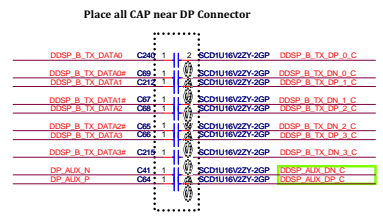
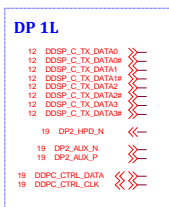


2012/10/11
Reserved EMI solution



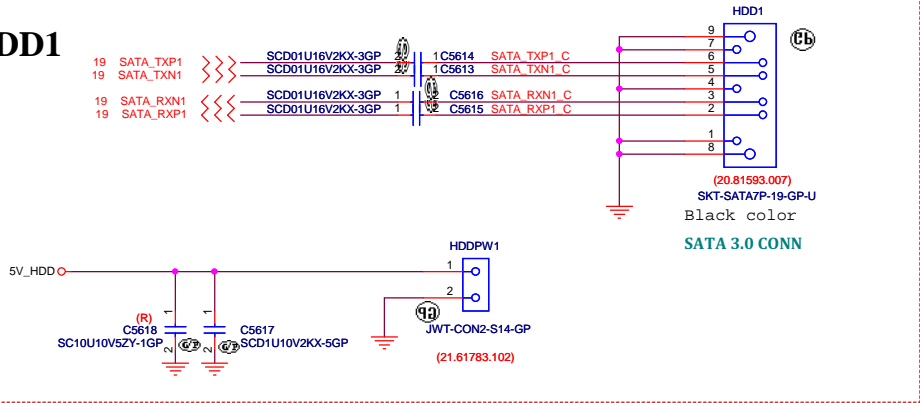
VGA



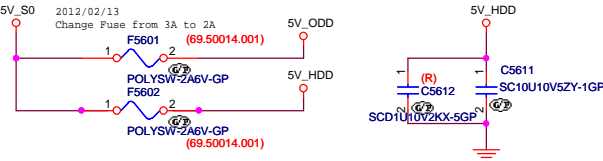


HDD Connector

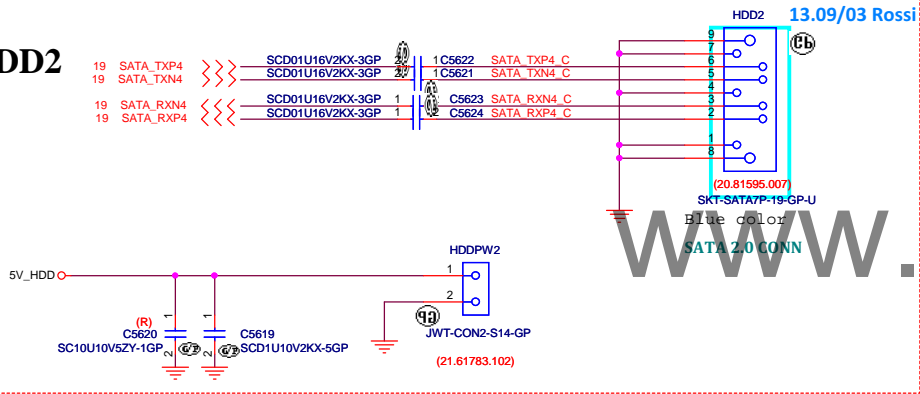
HDD1



Layout: Put them together

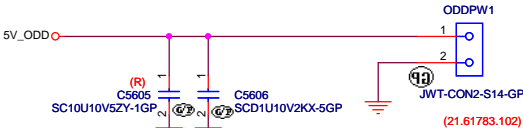
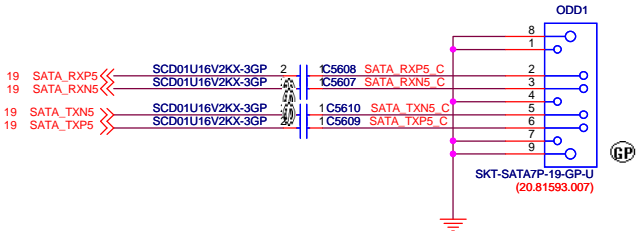


HDD2



13.09/03 Rossi Change to Blue color

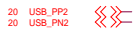
ODD Connector



USB3 Charger



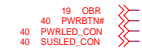
Card Reader



Audio



BTNB



HDD/LAN LED



ON/OFF

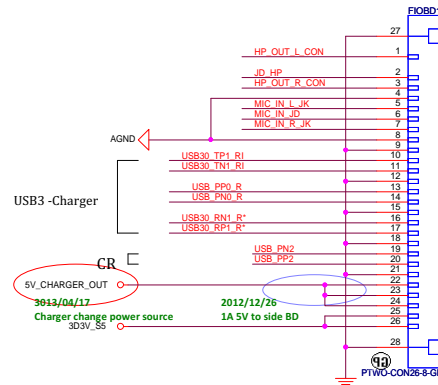
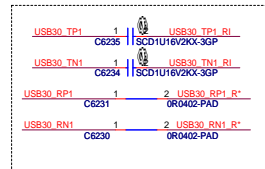


BRIGHTNESS



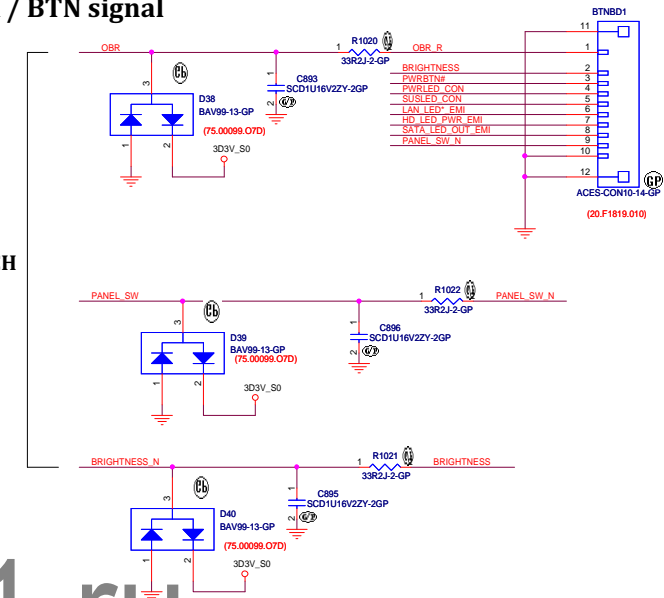
Side IO BD

2012/09/03
FFC1 (CR, USB3, Audio) 26pin



Button BD

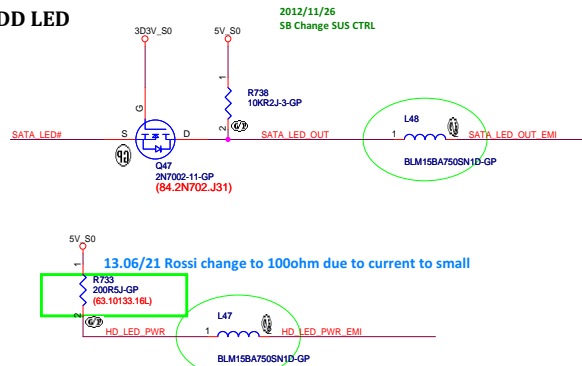
OBR / BTN signal



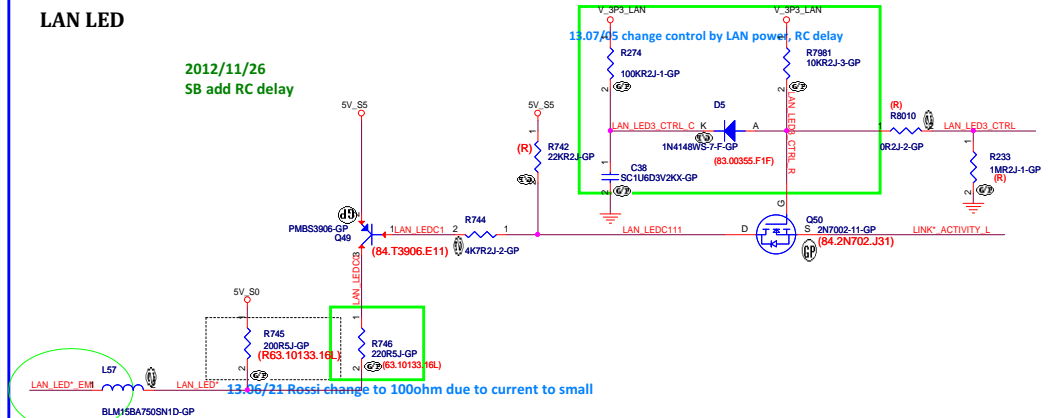
To PCH

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HDD LED



LAN LED



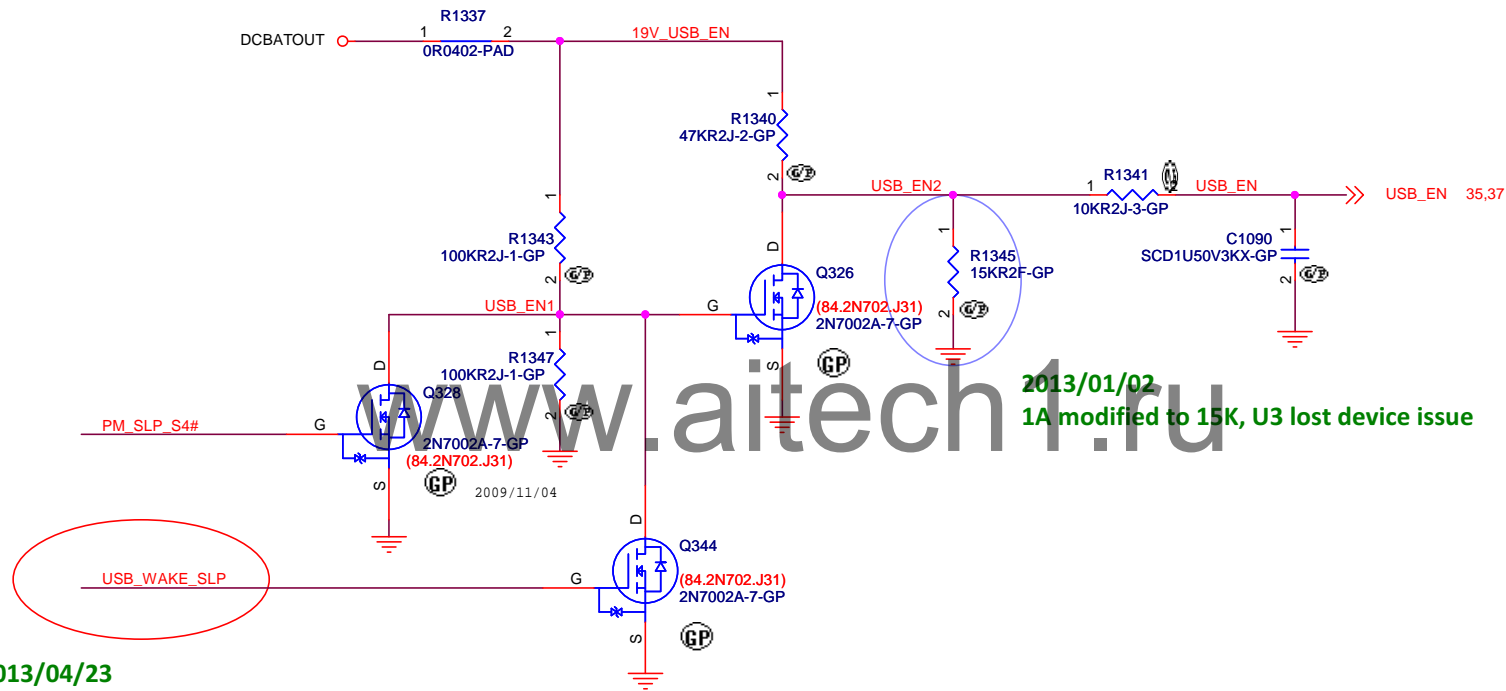
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File Side IO Port
Size C Document Number vSuperb
Date: Tuesday, October 08, 2013 Sheet 34 of 55
Rev -1

USB EN CTRL

17 USB_WAKE_SLP>>>———
17,24,53 PM_SLP_S4# >>>———



| | S5 | S4 | S3-S0 | | S5 | S4 | S3-S0 |
|--------------|----|----|-------|--------|----|----|-------|
| SLP_S4# | L | L | H | USB_EN | L | L | H |
| USB_WAKE_SLP | L | L | L | | H | H | H |
| USB_WAKE_SLP | H | H | H | | | | |

S4, S5 --> choice by USB_WAKE_SLP
S3-S0 --> choice by SLP_S4#

<Core Design>

| | | | |
|---------------------|---------------------------|---|-----|
| 緯創資通 | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| USB Power SW | | | |
| Size | Document Number | | Rev |
| Custom | vSuperb | | -1 |
| Date: | Tuesday, October 08, 2013 | Sheet 36 of 55 | |

WEBCAM

20 USB_PP11
20 USB_PN11

TOUCH

20 USB_PP9
20 USB_PN9

USB2.0

20 USB_OC_01

20 USB_PP8
20 USB_PN8

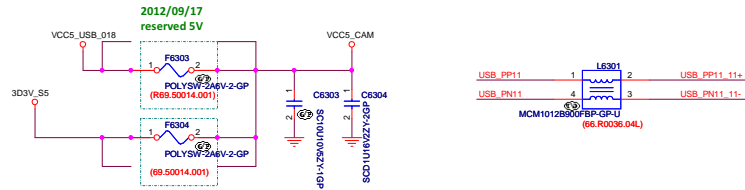
20 USB_PP3
20 USB_PN3

Reserved for 3L

20 USB_PP4
20 USB_PN4

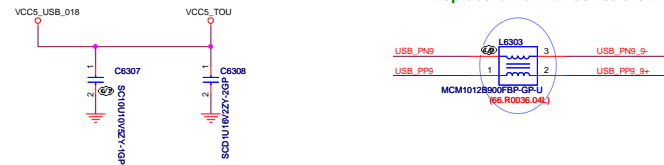
20 USB_PP5
20 USB_PN5

USB Port11 -> WEB CAM



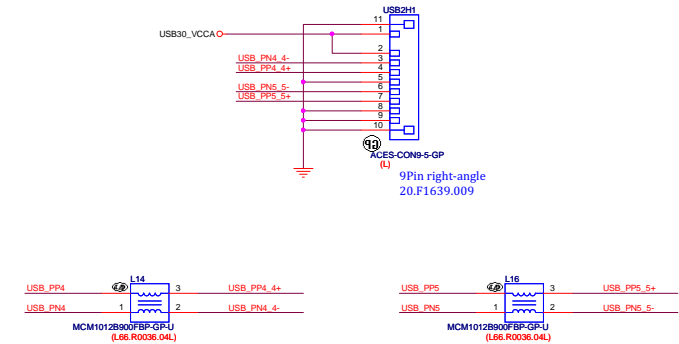
USB Port 9 -> TOUCH

2013/04/23
Replace CMC with series 0 Ohm

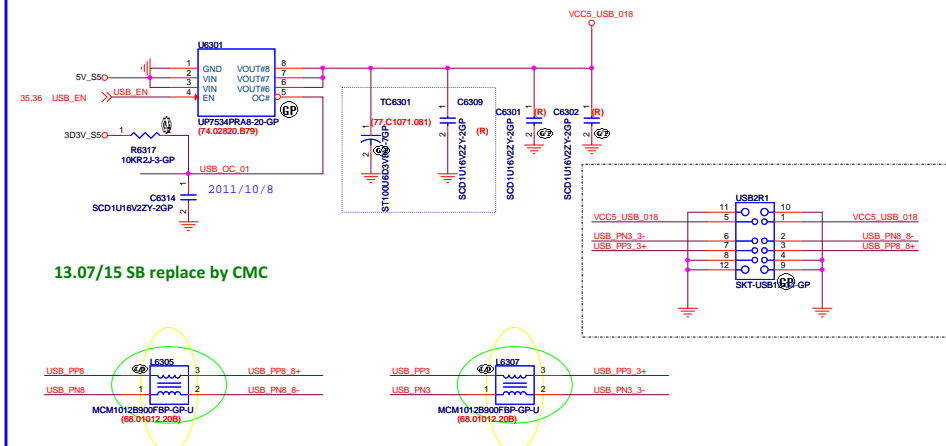


USB Port4,5 -> Reservd for 3L

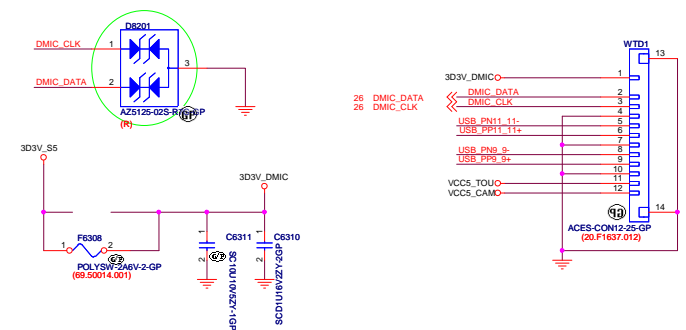
13.06/21 Rossi add Internal USB connector
power use rear USB3.0 power



USB Port 3,8-> REAR I/O



WEBCAM/TOUCH/DMIC Connector



<Core Design>

緯創資通 Wistron Corporation
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Taippei Hsien 301, Taiwan, R.O.C.

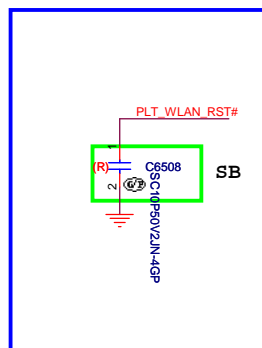
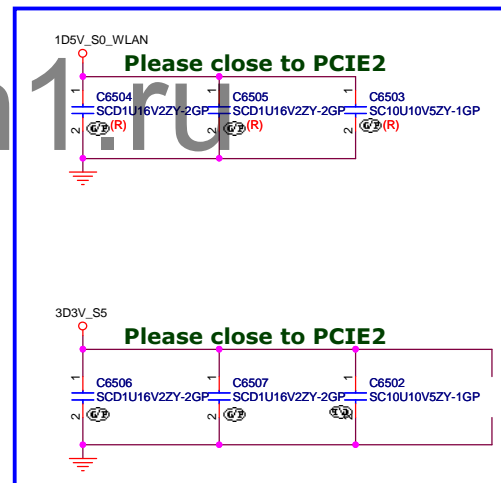
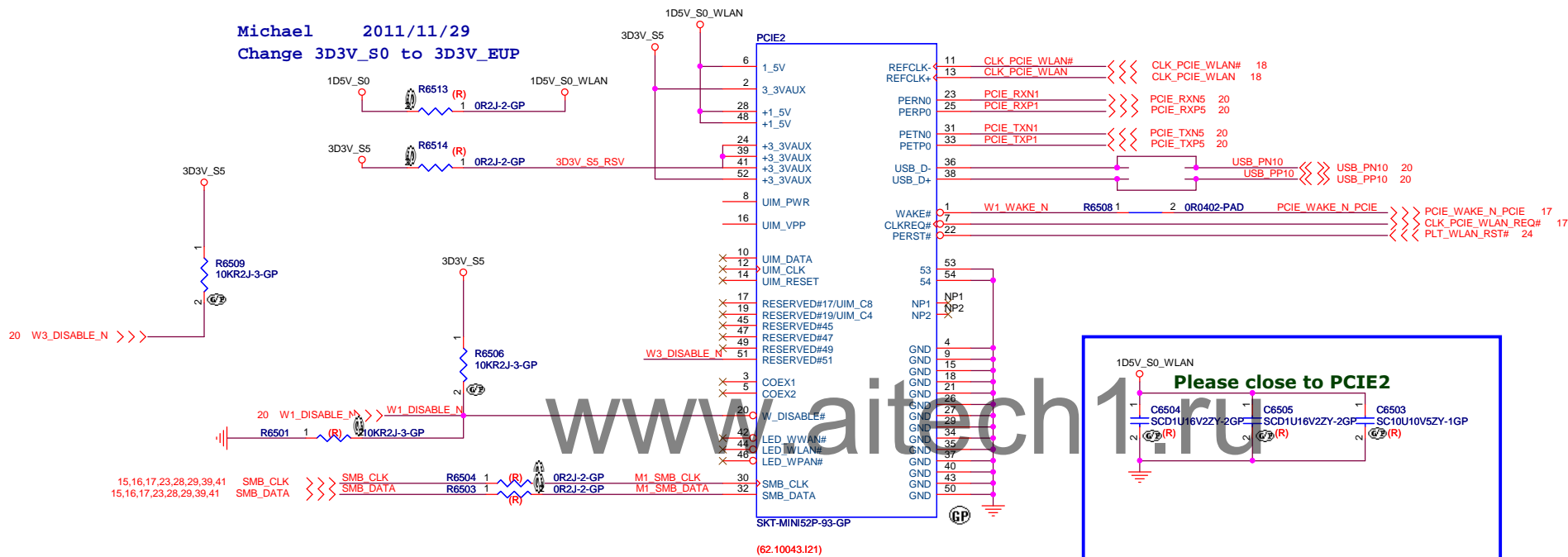
Title Rear USB/Touch/Web Cam
Size Document Number
Custom vSuperb
Date: Tuesday, October 08, 2013
Sheet 37 of 56
Rev -1

Mini Card Connector(Wireless LAN+BT)

Michael 2011/11/29
Change 1D5V_MEM to 1D5V_S0

Michael 2011/12/05
Change the MINI PCIE CONN P/N

Michael 2011/11/29
Change 3D3V_S0 to 3D3V_EUP



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| Title |
|-------|
|-------|

Mini PCIE WLAN/BT

| | |
|------|-----------------|
| Size | Document Number |
|------|-----------------|

Custom Document Number

Date: Tuesday, October 08, 2013

-1

vsSuperb

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mSATA

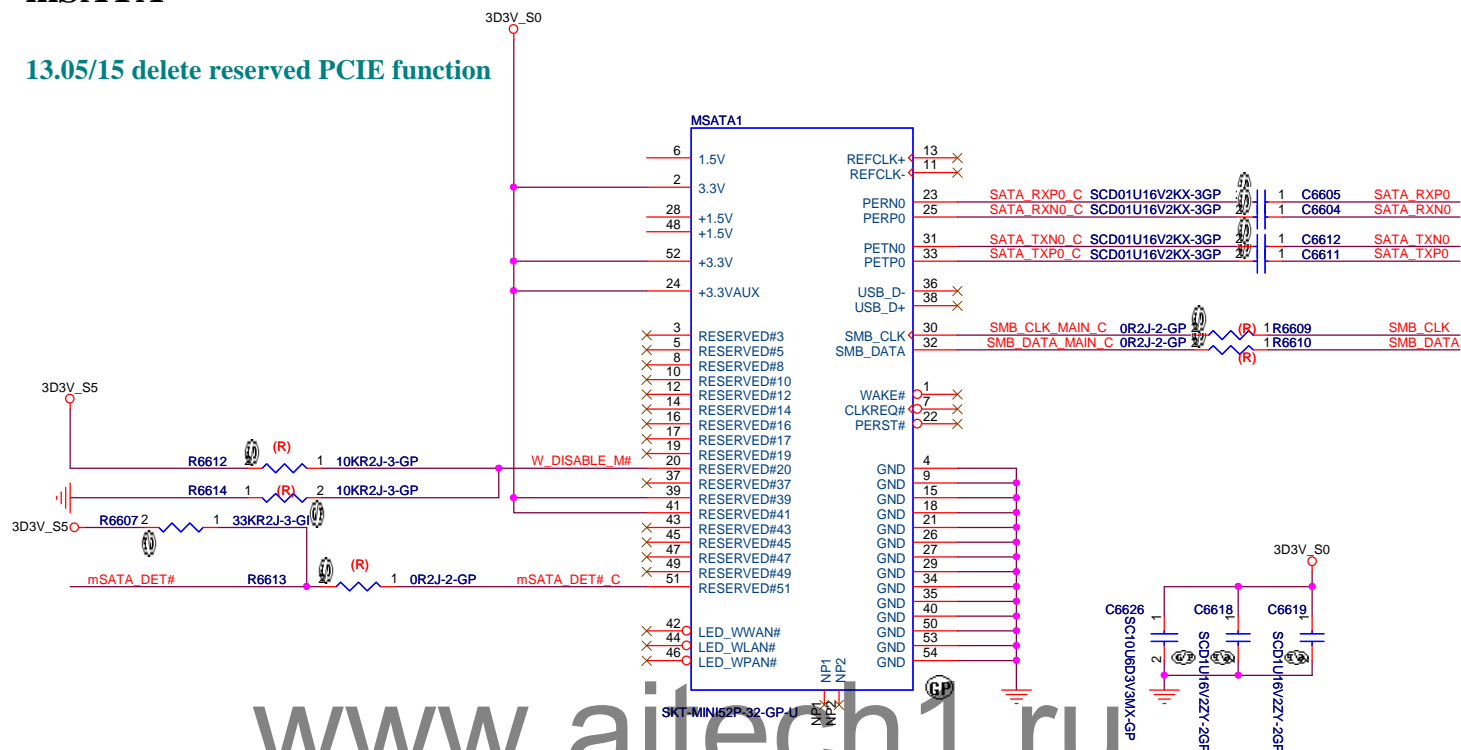
13.05/15 delete reserved PCIE function

SATA

19 SATA_RXP0
19 SATA_RXN0
19 SATA_TXN0
19 SATA_TXP0

Others

15,16,17,23,28,29,38,41 SMB_CLK
15,16,17,23,28,29,38,41 SMB_DATA
20 mSATA_DET#

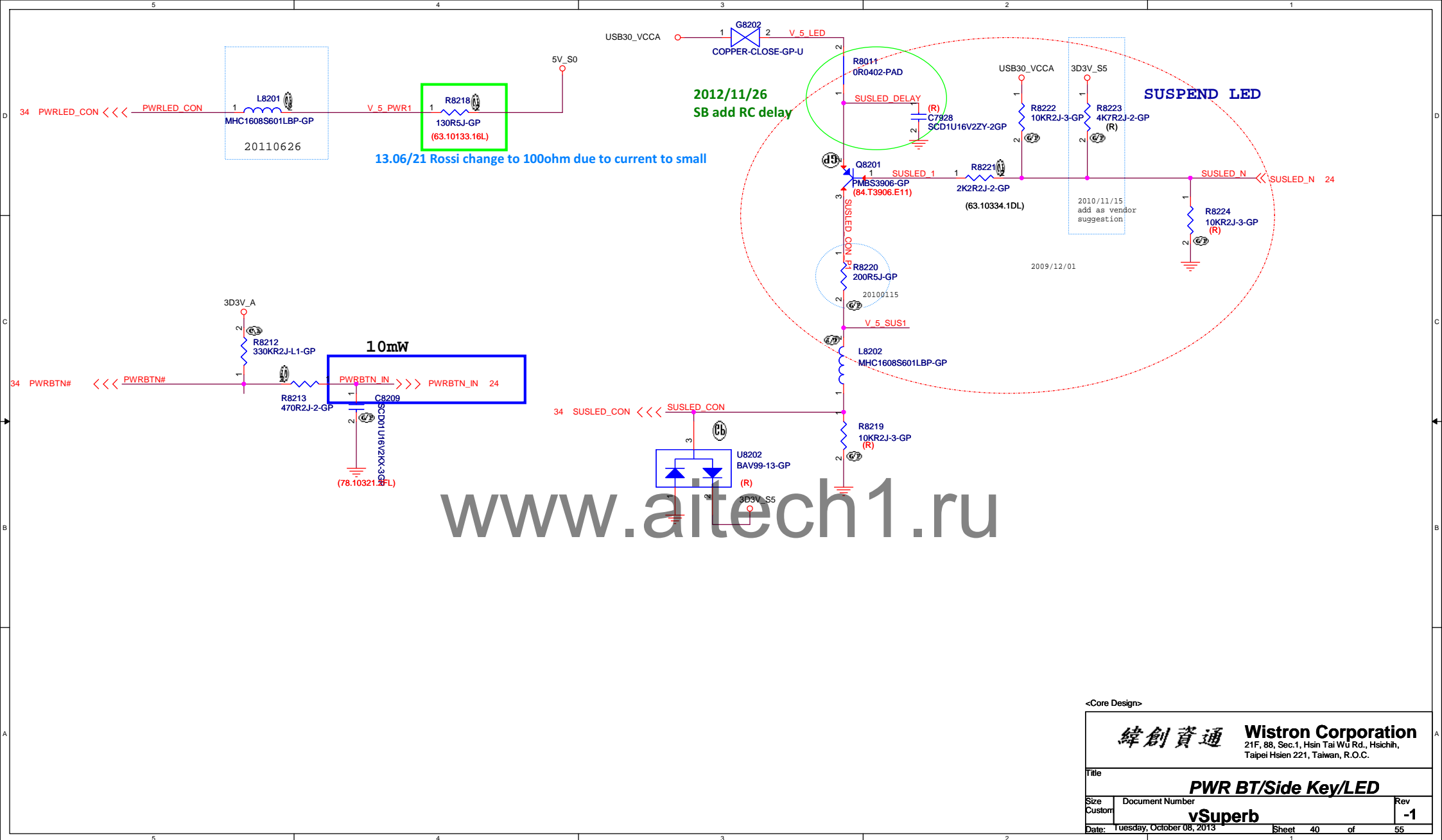


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Taipei Hsien 221, Taiwan, R.O.C.

| Title | | | |
|-----------------|---------------------------|---------|----------|
| Mini PCIE mSATA | | | |
| Size | Document Number | Rev | |
| Custom | | vSuperb | |
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Taipei Hsien 221, Taiwan, R.O.C.

Title

PWR BT/Side Key/LED

Size
Custom

Document Number

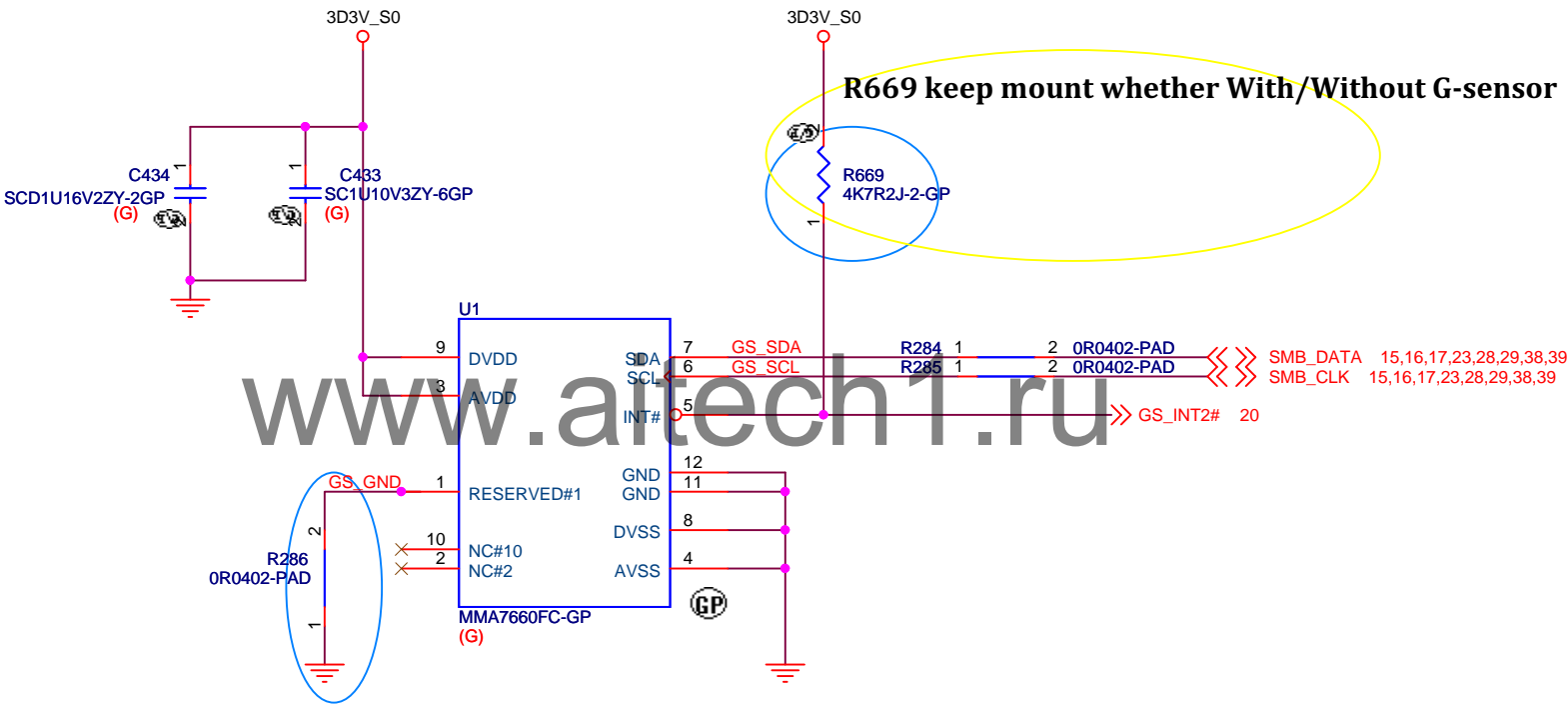
vSuperb

Rev
-1

Date: Tuesday, October 08, 2013

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G-Sensor



<Core Design>

| | | | |
|-----------------|-----------------------------------|---|------------------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| G-Sensor | | | |
| Size A4 | Document Number vSuperb | | Rev -1 |
| Date: | Tuesday, October 08, 2013 | Sheet 41 of | 55 |

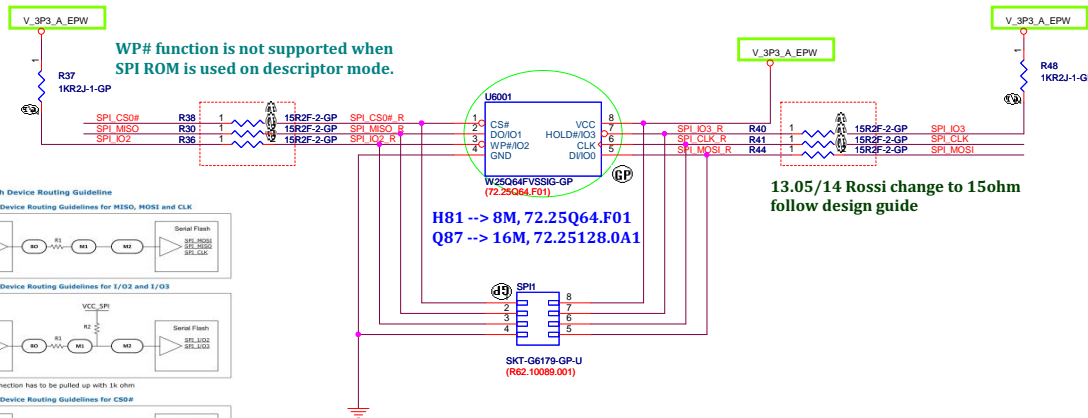
SPI

17 SPI_CS0#
17 SPI_MISO
17 SPI_IO2
17 SPI_CLK
17 SPI_MOSI
17 SPI_WP_R_N

17,54 PCH_SLP_A

SPI ROM Equal length need to less than 500mil

WP# function is not supported when SPI ROM is used on descriptor mode.



2013/05/08
Rossi Delete BIOS WP header

22.3.1.1 SPI Single Flash Device Routing Guideline

Figure 22-2. SPI Single Flash Device Routing Guidelines for MISO, HOLD and CLK

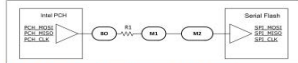
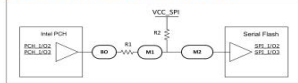
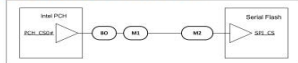


Figure 22-3. SPI Single Flash Device Routing Guidelines for I/O2 and I/O3



Note: I/O2 and I/O3 connection has to be pulled up with 1k ohm

Figure 22-4. SPI Single Flash Device Routing Guidelines for CS#

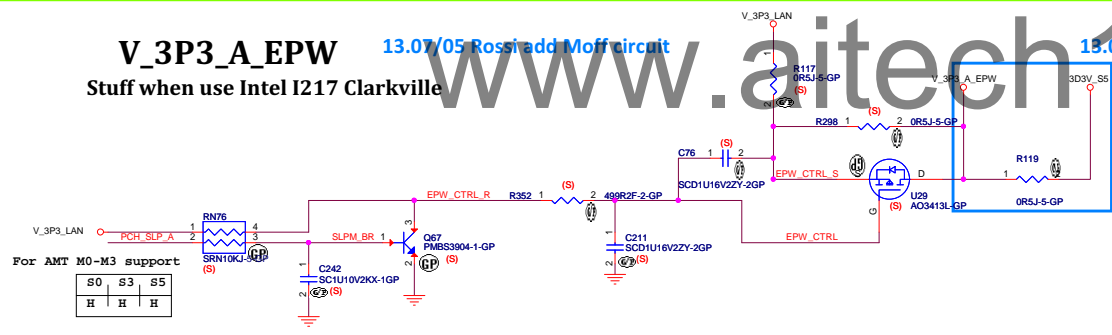


| | | | |
|--------|----|-----|----|
| Signal | R1 | pin | 1k |
| | R2 | pin | 1k |

V_3P3_A_EPW
Stuff when use Intel I217 Clarkville

13.07/05 Rossi add Mof circuit

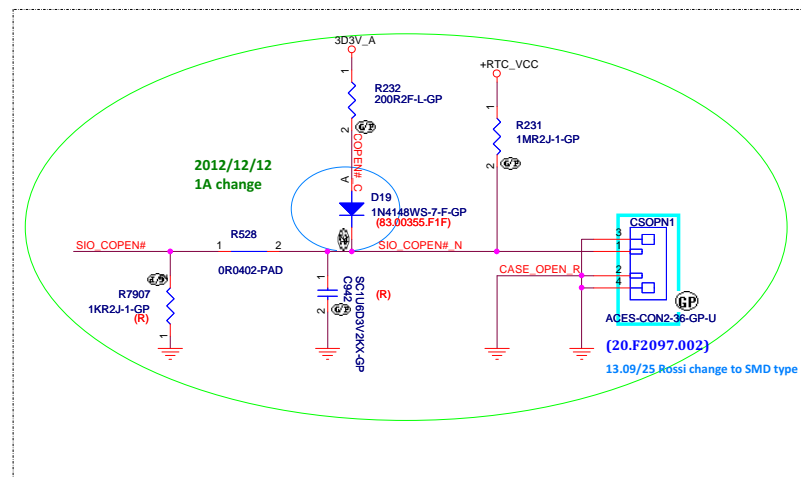
13.07/06 V_3P3_A_EPW = 3D3V_S5



Chassis Intrusion

2012/11/26

SB case open follow SIO suggest

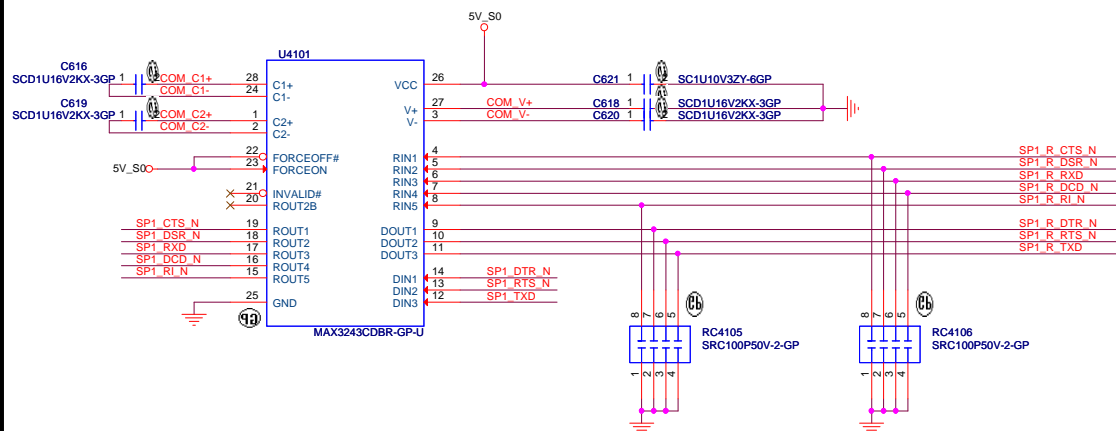


2012/09/18

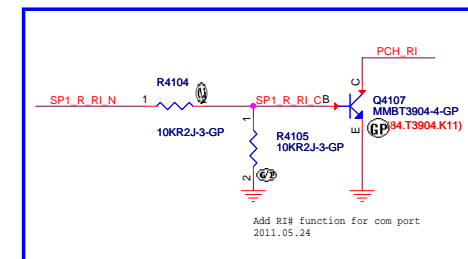
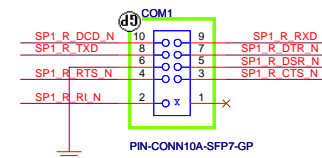
Rossi add Com port header

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SERIAL PORT



13.07/05 Change comport to 2.0 pitch type



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| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
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CSOPN/COM Port

Size

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| Document Number |
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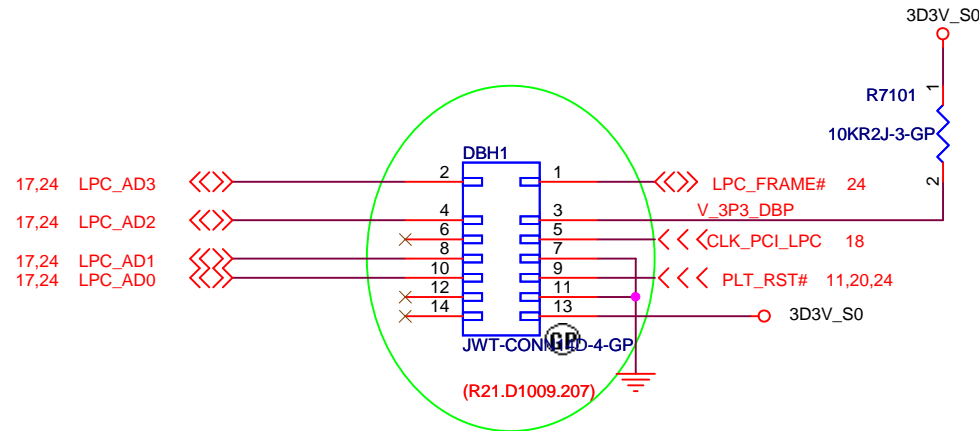
vSuperb

Rev

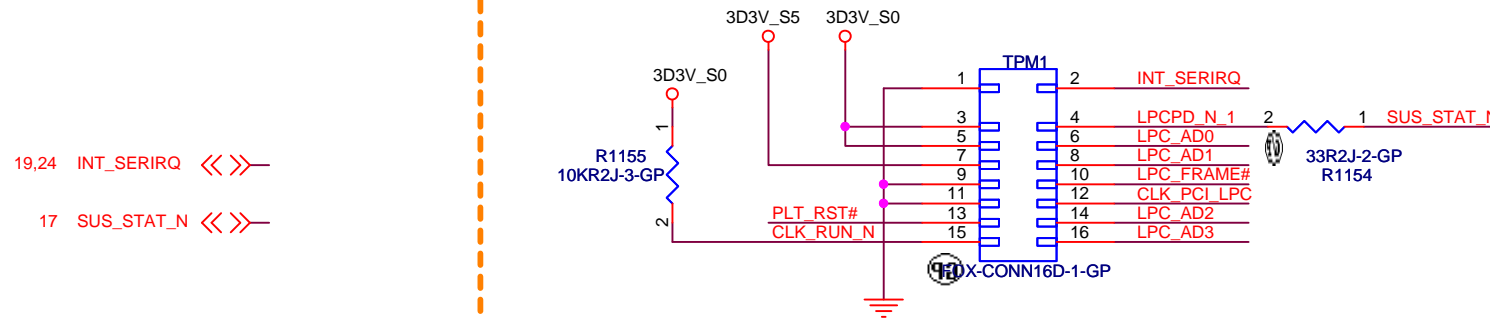
Date: Tuesday, October 08, 2013

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TPM Header (v MARR) www.aitech1.ru

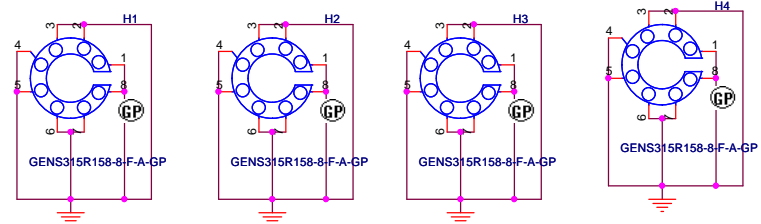


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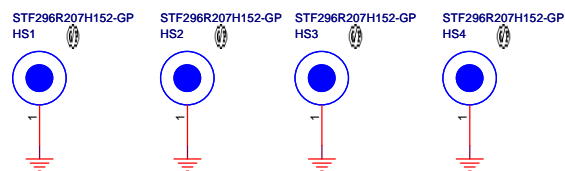
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | | |
|-------|---------------------------|--|-----------------------|----------|
| Title | | | Debug connector / TPM | |
| Size | Document Number | | Rev | |
| A4 | vSuperb | | -1 | |
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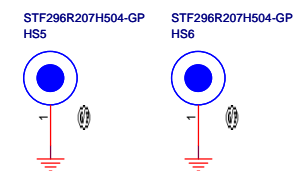
MB Screw



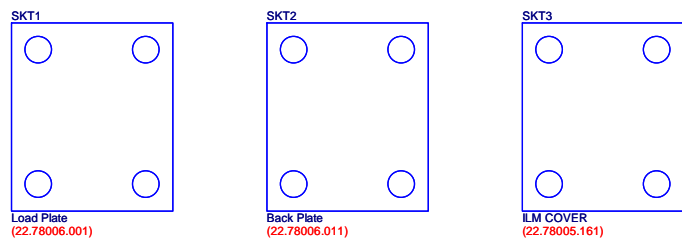
CPU



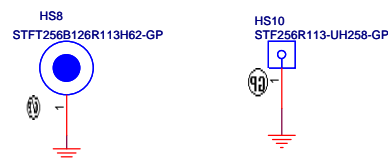
CPU FAN



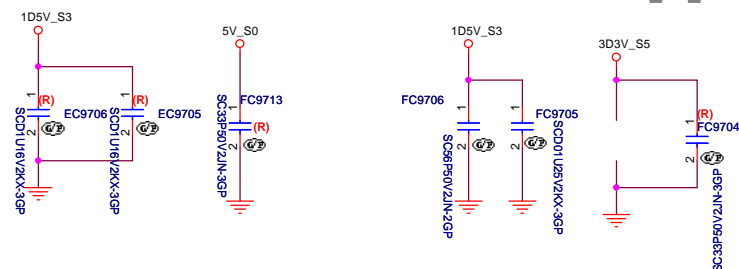
CPU Plate



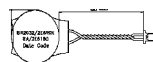
mSATA/WIFI



EMI



Battery



BAT1
BATTERY CR2032_30MM
(23.21221.024)
Wire Length: 30mm

Vendor
P/N:
23.21221.024
23.21212.031

LABEL



LBL1
LABEL
(40.3KP03.001)

MB serial NO# and MAC address
45.41101.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm

<Core Design>

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Title

Dummy Symbol/EMI CAP

Size

Document Number

Rev

Date

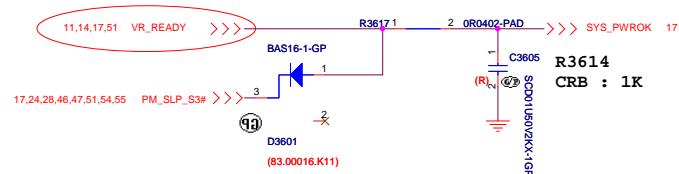
Tuesday, October 08, 2013

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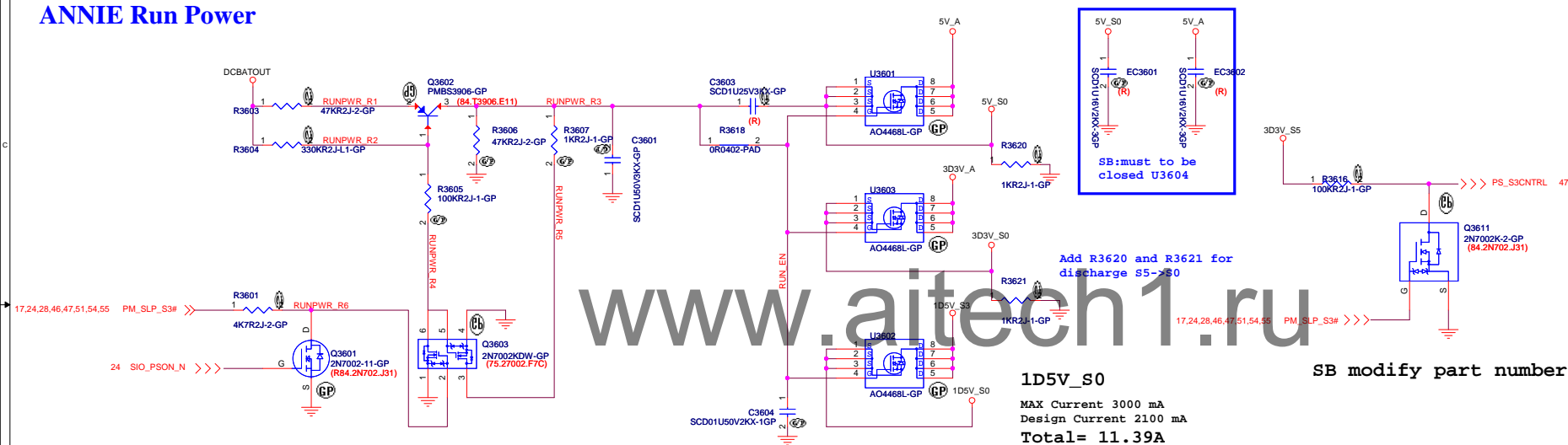
vSuperb

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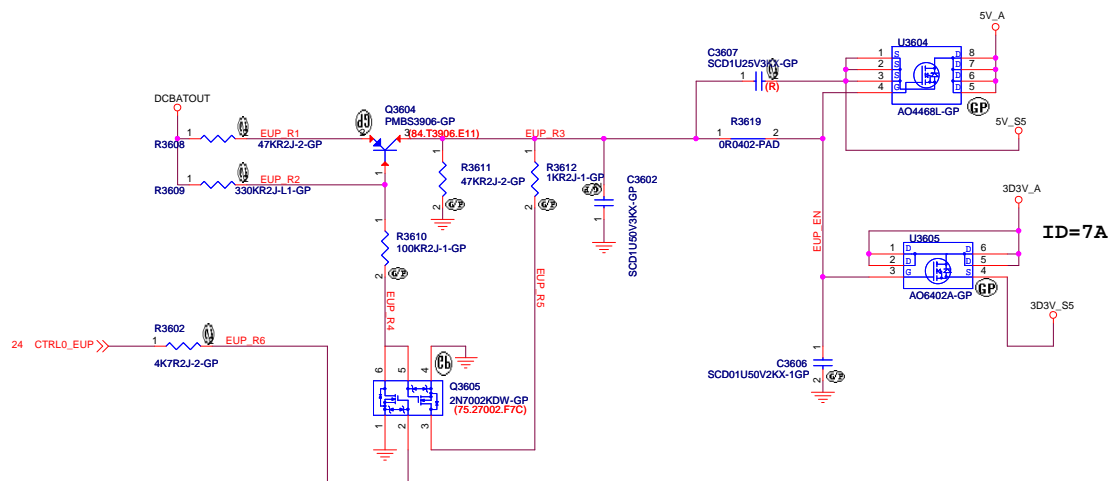
Power Sequence



ANNIE Run Power



EUP Power

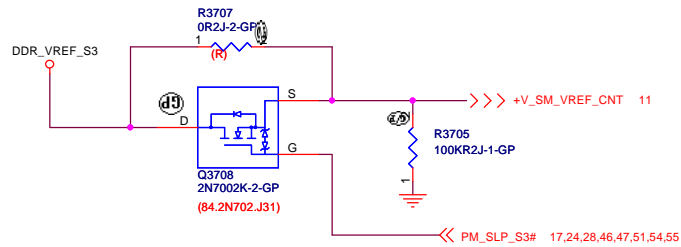


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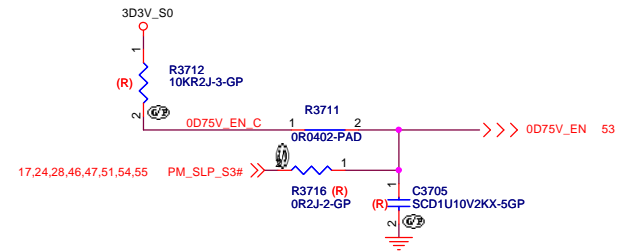
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|------------------------------------|---------------------------|--|----------------|
| Title | | | |
| <i>Run Power / Sequence</i> | | | |
| Size | Document Number | | Rev |
| Custom | vSuperb | | -1 |
| Date: | Tuesday, October 08, 2013 | | Sheet 46 of 55 |

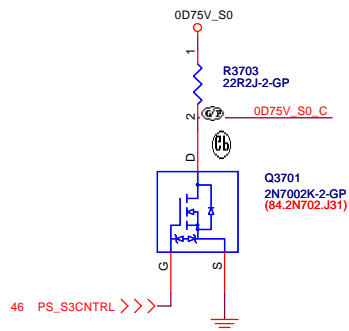
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



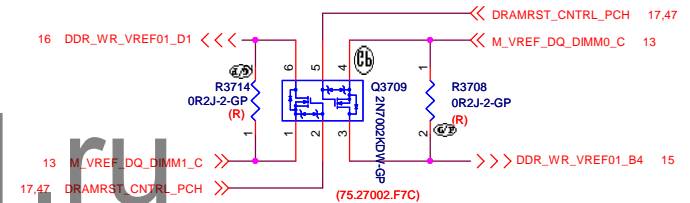
⑤ S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件



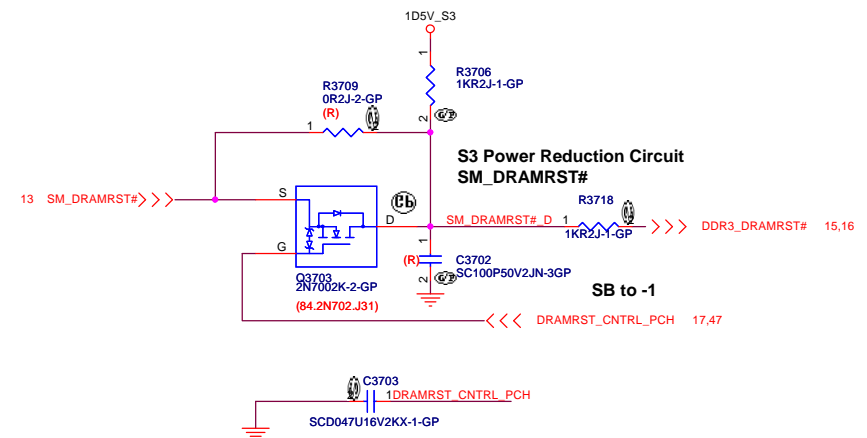
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



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Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



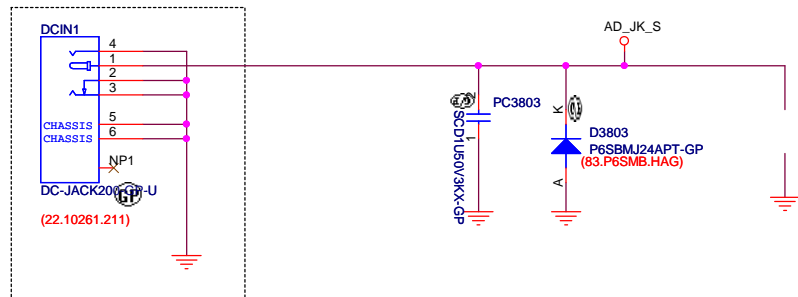
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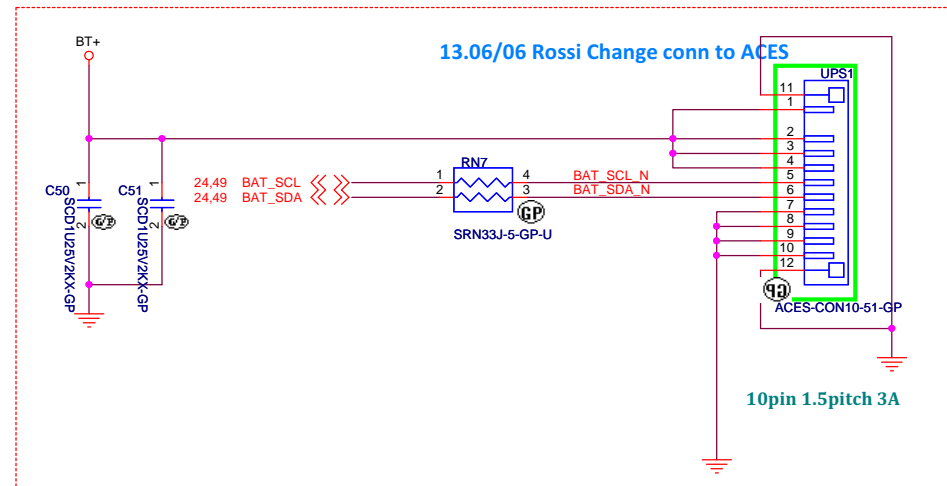
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|---------------------------------|-----------------|-----|----------------|
| Title | | | ADAPTER OCP |
| Size | Document Number | Rev | |
| A3 | | -1 | |
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SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

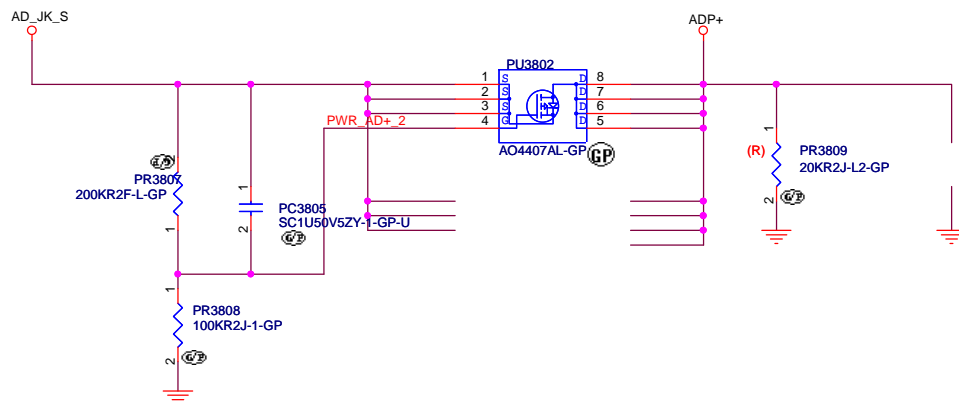
ANNIE solution



BATTERY CONN



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Title

DCIN JACK

Size

Document Number

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Rev

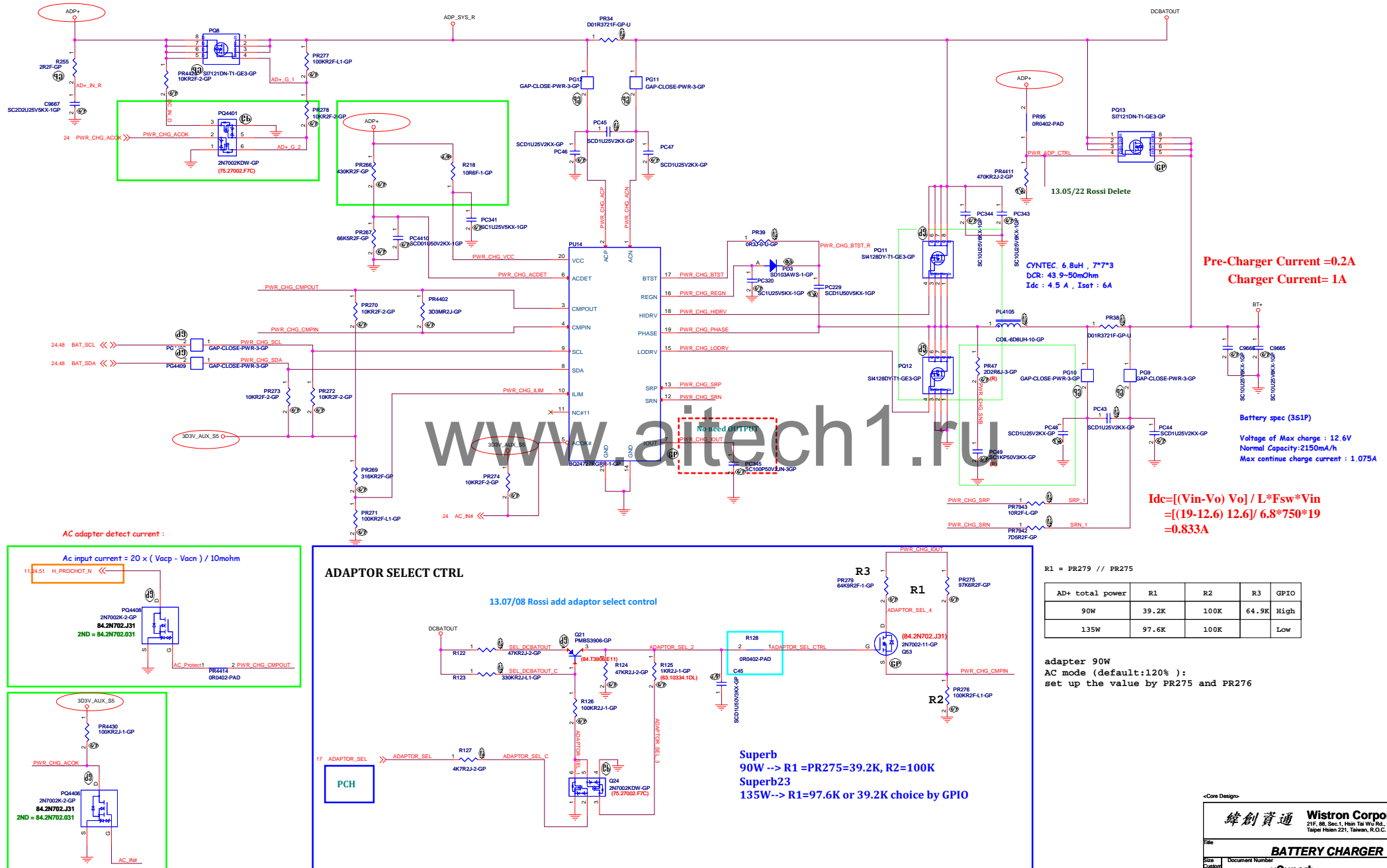
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Date: Tuesday, October 08, 2013

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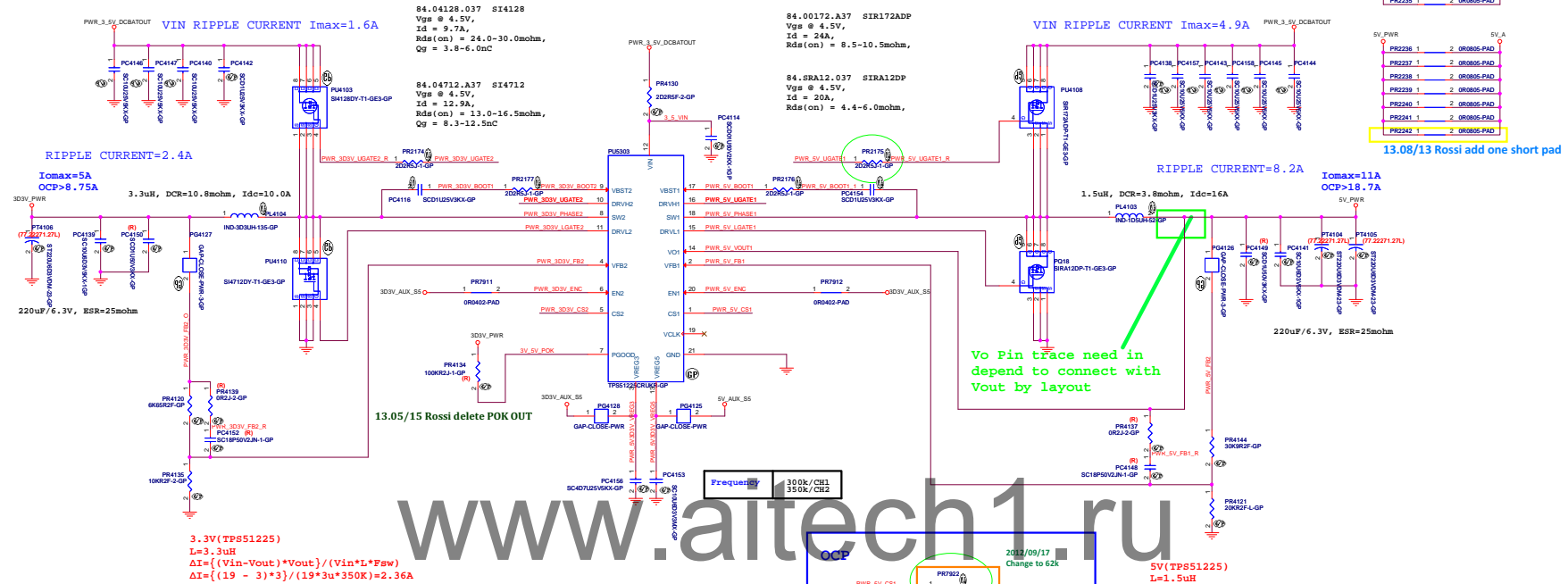
of 55

BATTERY CHARGER





3D3V_PWR / 5V_PWR



| TONESEL | CH1 | CH2 |
|-----------------|--------|--------|
| GND | 200KRs | 250KRs |
| VREF | 300KRs | 375KRs |
| PRB23 or VREF25 | 400KRs | 500KRs |

| SKIPSEL | VREF03 or VREF05 | VREF(2V) | GND |
|----------------|------------------|-----------|----------|
| Operating Mode | OC Auto Skip | Auto Skip | PWM only |

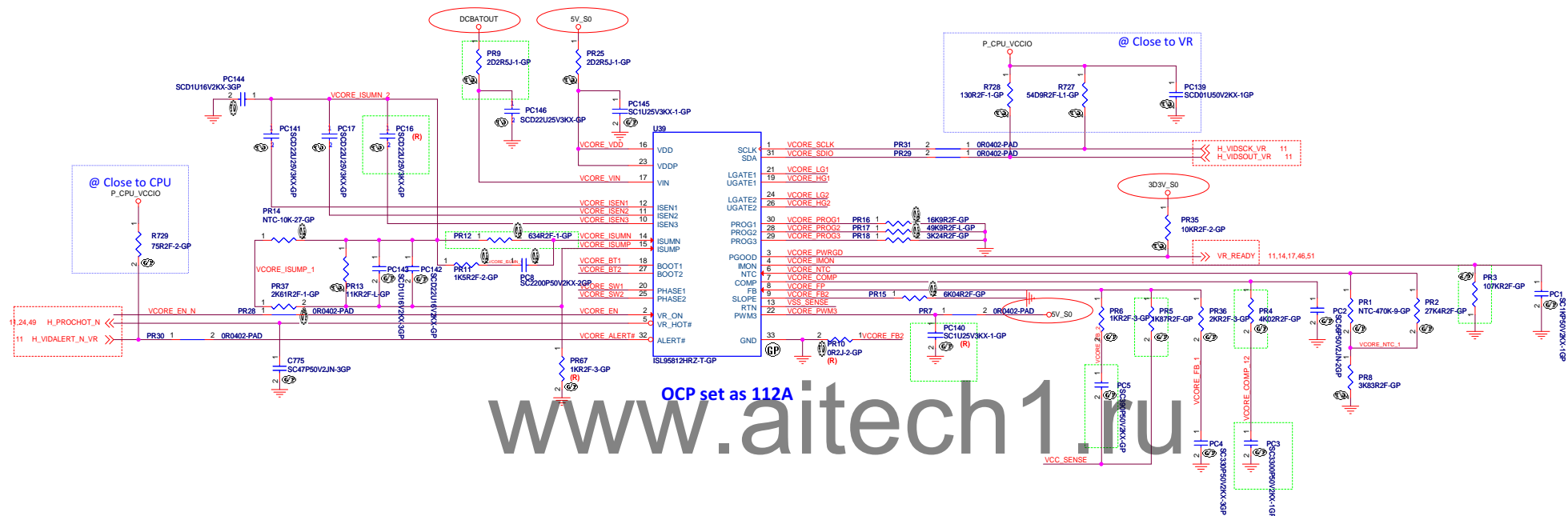
PWM only

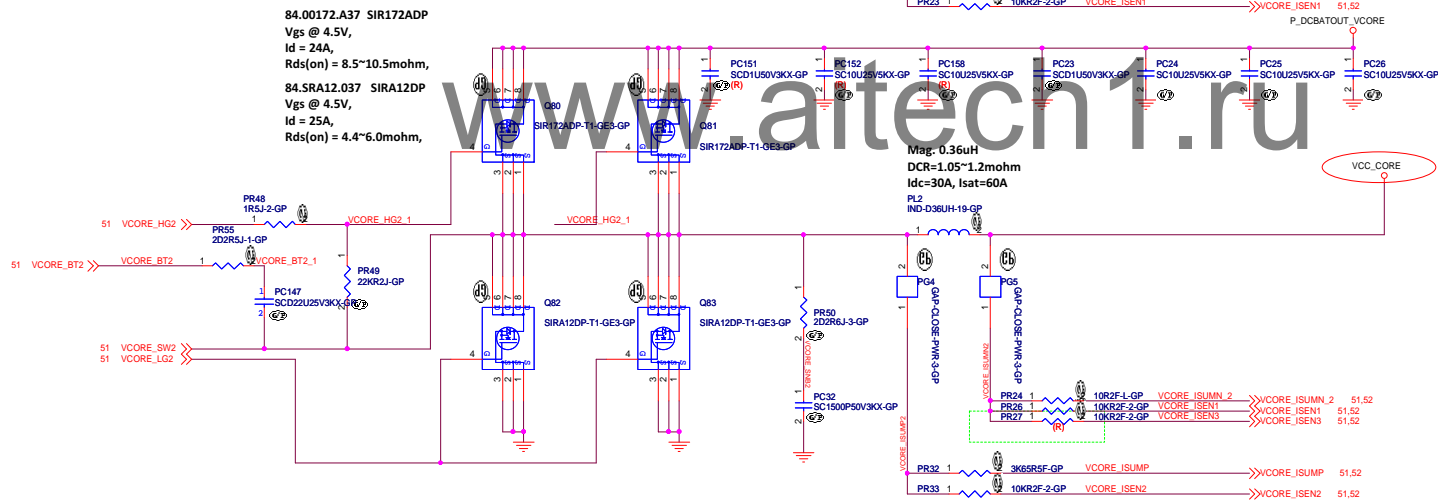
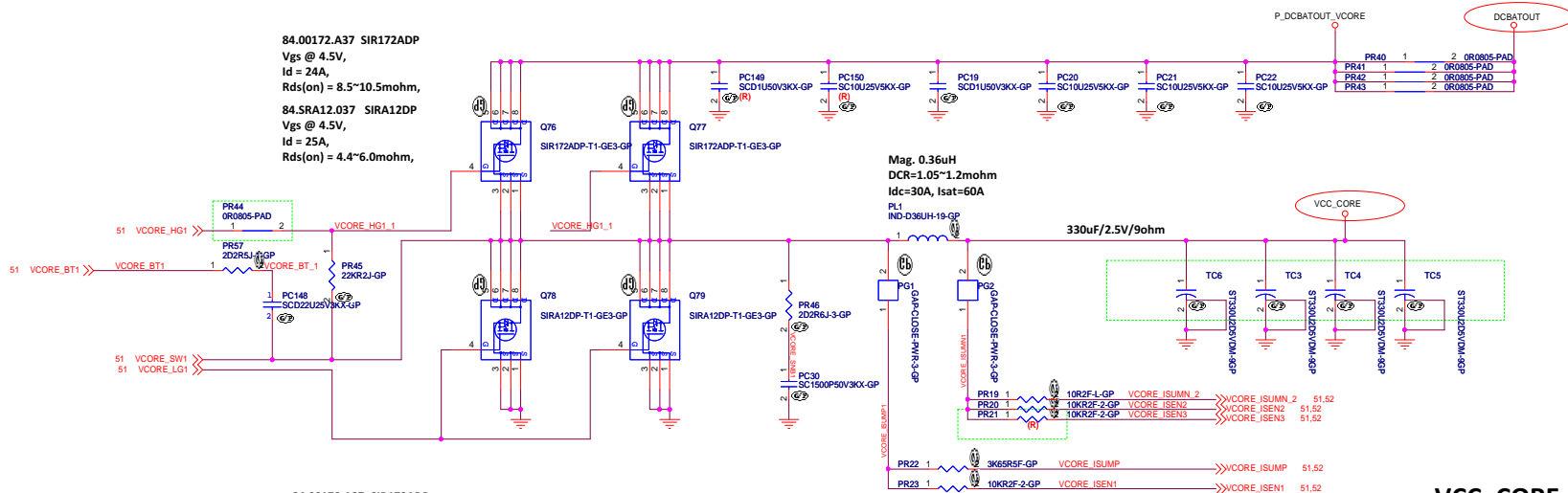
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File
5V3D3V(TPS51125)
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VCORE_SW2 >>>VCORE_SW2 52
VCORE_SW1 >>>VCORE_SW1 52
VCORE_BT1 >>>VCORE_BT1 52
VCORE_BT2 >>>VCORE_BT2 52
VCORE_LG1 >>>VCORE_LG1 52
VCORE_HG1 >>>VCORE_HG1 52
VCORE_LG2 >>>VCORE_LG2 52
VCORE_HG2 >>>VCORE_HG2 52
VCORE_ISEN1 >>>VCORE_ISEN1 52
VCORE_ISEN2 >>>VCORE_ISEN2 52
VCORE_ISEN3 >>>VCORE_ISEN3 52
VCORE_ISUMP >>>VCORE_ISUMP 52
VCORE_ISUMN_2 >>>VCORE_ISUMN_2 52





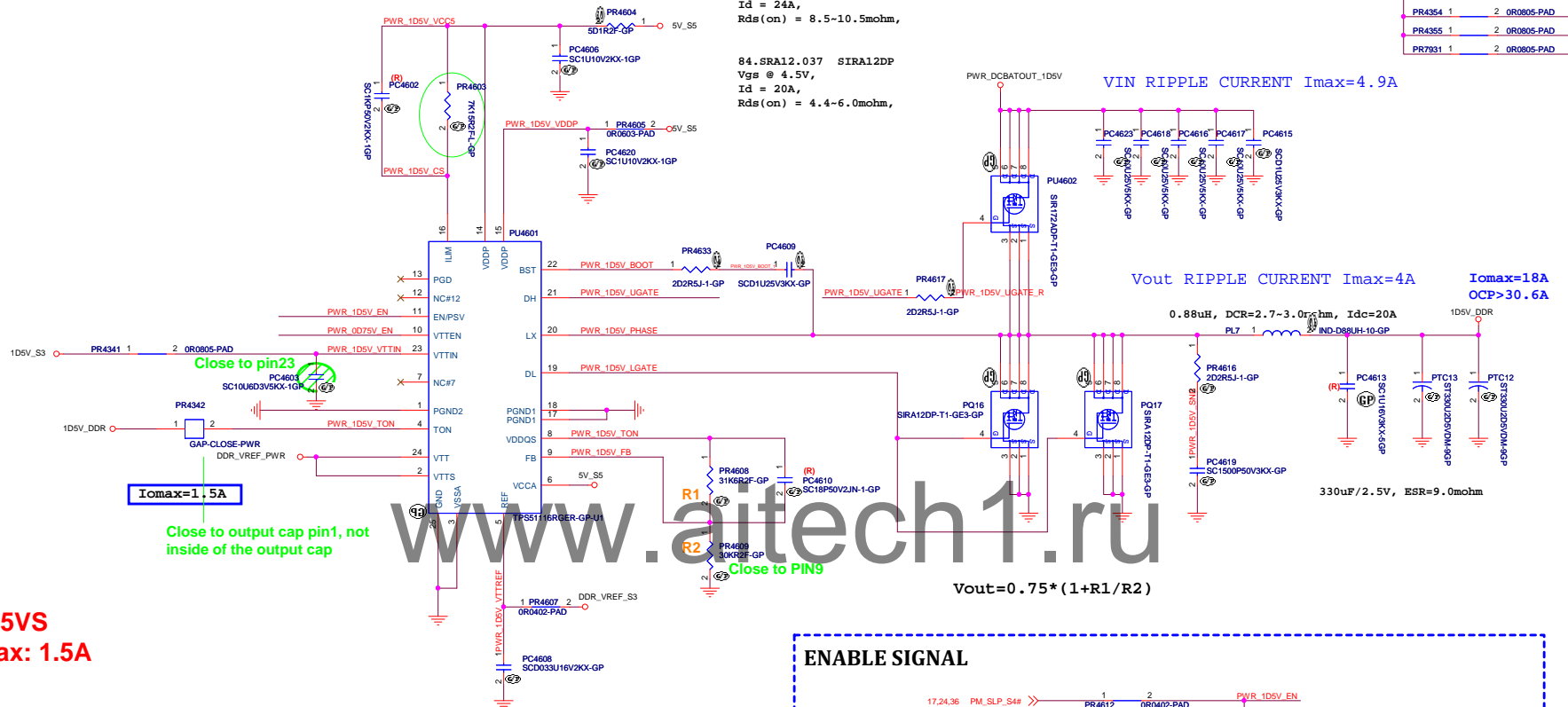
VCC_CORE
Tdc=26A Iomax=58A (45W)
Tdc=20A Iomax=48A (35W)

<Core Design>

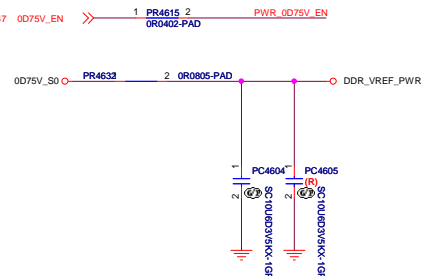
TPS51116 for 1D5V

84.00172.A37 SIR172ADF
Vgs @ 4.5V,
Id = 24A,
Rds(on) = 8.5~10.5mohm,

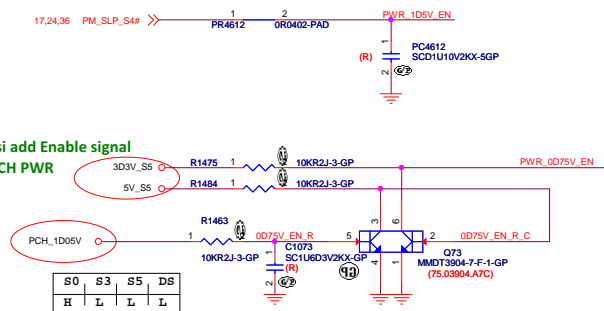
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



+0.75VS
Iomax: 1.5A



ENABLE SIGNAL



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

| Title | Author | Date | Page |
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| 1. Introduction | John Doe | 2023-10-27 | 10 |
| 2. Methodology | John Doe | 2023-10-27 | 15 |
| 3. Results | John Doe | 2023-10-27 | 20 |
| 4. Discussion | John Doe | 2023-10-27 | 25 |
| 5. Conclusion | John Doe | 2023-10-27 | 30 |

1D5V/0D75V(TPS51116)

Size
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Document Number **vSuperb**

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1D05V_ME
(APL5930)

19 POH_MEPWROK <<-

